

Project Namel: Red Skull Bristol
PCB Number: 16542-1
PCBA Ver.: A00
SCH Ver.: A00
Project Code: 3PD08C010001
PCB Size: 244*244mm

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09	AM4_VSS
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11	AM4_Power_CAP2
12	Hardwave Strap
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14	DDR4_CHB_DIMM_0
15	(R)
16	(R)
17	PROMONTORY_PCIE/SATA
18	PROMONTORY_GPIO
19	PROMONTORY_USB/CLK
20	PROMONTORY_Power
21	PROM_Power_CAP
22	(R)
23	(R)
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25	Flash&RTC
26	FAN_CCTRL/HOLE
27	AUDIO_(ALC3861)
28	(R)
29	AUDIO_Rear_IO
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32	RJ45+USB_Port
33	Rear_KB&MS
34	Rear_USB3.0_Port
35	(R)
36	Front_SD4.0_Header
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38	Front_USB3.0_w/CR_Header
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46	Vcore_CPU_ISL6377(2-1)
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49	1D05V_VDDP_S5_AOZ2262
50	1D2V_VDDQ_RT8231A
51	0D775V_S5_APL5337
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PAGE	TITLE
56	HDMI_Retimer
57	(R)
58	(R)
59	(R)
60	HDD/ODD
61	M.2_WLAN_Key_A
62	M.2_SSD_Key_M
63	(R)
64	PWR_BTN/LED
65	(R)
66	(R)
67	(R)
68	LPC/UART_Port
69	(R)
70	(R)
71	TYPE-C_PD
72	(R)
73	(R)
74	(R)
75	(R)
76	(R)
77	(R)
78	(R)
79	(R)
80	(R)
81	(R)
82	(R)
83	(R)
84	(R)
85	(R)
86	(R)
87	(R)
88	(R)
89	(R)
90	(R)
91	TPM
92	(R)
93	PCIE_x16_SLOT1
94	PCIE_x16_SLOT4
95	PCIE_x1_SLOT2_3
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97	(R)
98	(R)
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101	(R)
102	Power_Sequence
103	Power_Block_Diagram
104	Power_Sequence_Diagram
105	Clock_Map
106	Reset_Flow_Chart
107	Change_Histroy

Jumper Setting

JMP1	Pin 1-2	With Jumper to Service Mode
	Pin 3-4	Without Jumper to Clear Password
	Pin 5-6	With Jumper to Clear CMOS

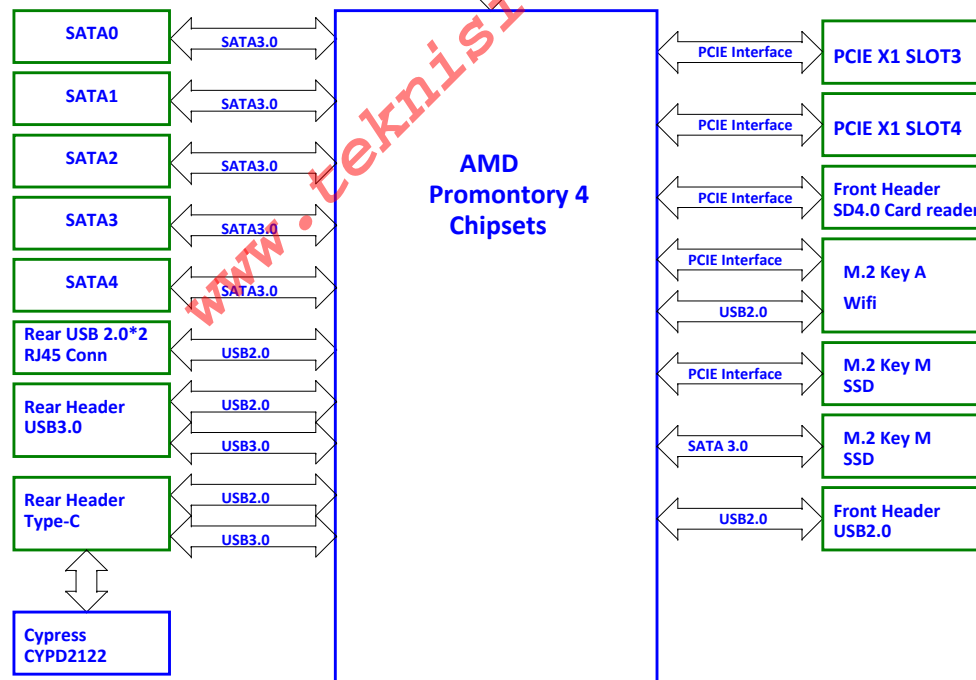
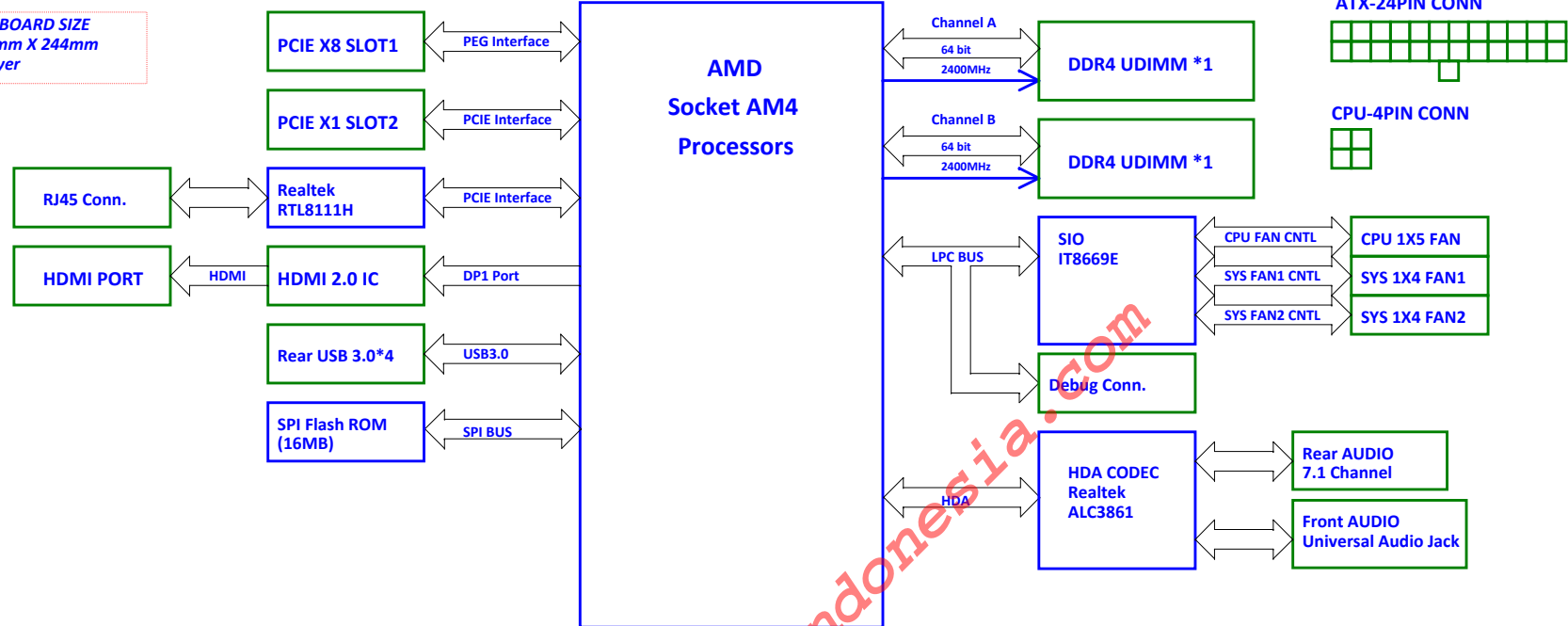
BOM Configuration

(R): Unmount
(X): Debug
(T): TPM

Power sates

	Name	G3	EuP	S5	S4	S3	S0
+12V	12V_S0						O
	12V_CPU_S0						O
-12V	-12V_S0						O
	5V_S0						O
+5V	5V_S5						
	5V_KBMS						
	5V_USBR1						
	5V_USBR2						
	5V_USBR3			O	O	O	O
	5V_USBPD						
	5V_USBF1						
	5V_USBF2						
	5V_USB_CHAR						
	5V_LPS						
3.3V	5V_CODECD		O	O	O	O	O
	5V_AUD_LDO						
	3D3V_S0						
	3D3V_AUD_S0						
	3D3V_S0_SOC						O
	3D3V_S0_PCH						
	3D3V_S5						
	3D3V_S5_PCH						
	3D3V_LAN			O	O	O	O
	3D3V_WLAN						
VBAT	3D3V_VDDPD						
	3D3V_LPS		O	O	O	O	O
	3V_VBAT1						
	3V_VBAT2	O	O	O	O	O	O
	3D3V_RTC						
	1D5V_VBAT_AUX						
	1D5V_VDDBT_RTC	O	O	O	O	O	O
	1D2V_VDDIO_MEM						
	2D5V_MEMVFP_S5					O	O
	DDR_VTT						O
FCH	2D5V_S0_PVH						O
	1D05V_S0_PCH						
	1D05V_S5			O	O	O	O
CPU	1V_VDDCR_CPU						
	1V_VDDCR_SOC						
	1D05V_VDDP_S0						O
	1D8V_S0						
	1D05V_VDDP_S5						
	VDDCR_SOC_S5			O	O	O	O
	1D8V_S5						
	1D5V_S5						

PCB BOARD SIZE
244mm X 244mm
4 Layer



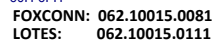
[17] DMI_RX_CPU_P[0..3] <<>>
[17] DMI_RX_CPU_N[0..3] <<>>

[17] DMI_TX_CPU_P[0..3] <<>>
[17] DMI_TX_CPU_N[0..3] <<>>

[93] PEG_TX_CPU_P[0..7] <<< 
 [93] PEG_TX_CPU_N[0..7] <<< 
 [93] PEG_RX_CPU_P[0..7] >>> 
 [93] PEG_RX_CPU_N[0..7] >>> 

```
[95] PCIE_TX_CPU_P0 <--
[95] PCIE_TX_CPU_N0 <--
[95] PCIE_RX_CPU_P0 >--
[95] PCIE_RX_CPU_N0 >--

[31] PCIE_TX_CPU_P1 <--
[31] PCIE_TX_CPU_N1 <--
[31] PCIE_RX_CPU_P1 >--
[31] PCIE_RX_CPU_N1 >--
```



LAN

P0A, P0B:
Only supported on AM4 Type 2 processor



Date: Friday, March 10, 2017 Sheet 3 of 107

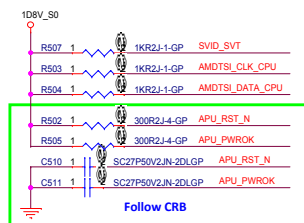
[13]	M_A_DQS_0[0..63]	<<	>>
[13]	M_A_DQS_DmQ0..7	<<	>>
[13]	M_A_DQS_DmQ0..7	<<	>>
[13]	M_A_A0[-13]	<<	>>
[13]	M_A_B00	<<	>>
[13]	M_A_BG1	<<	>>
[13]	M_A_A17	<<	>>
[13]	M_A_DmQ0..7	<<	>>
[13]	M_A_CKE0	<<	>>
[13]	M_A_CKE1	<<	>>
[13]	M_A_CS0..N	<<	>>
[13]	M_A_CS1..N	<<	>>
[13]	M_A_ODT0	<<	>>
[13]	M_A_ODT1	<<	>>
[13]	M_A_BA0	<<	>>
[13]	M_A_BA1	<<	>>
[13]	M_A_CLK0_P	<<	>>
[13]	M_A_CLK0_N	<<	>>
[13]	M_A_CLK1_P	<<	>>
[13]	M_A_CLK1_N	<<	>>
[13]	M_A_DRAMRST_N	<<	>>
[13]	M_A_A16_WE_N	<<	>>
[13]	M_A_A16_OAS_N	<<	>>
[13]	M_A_A16_RAS_N	<<	>>
[13]	M_A_ACT_N	<<	>>
[13]	M_A_EVENT_N	<<	>>
[13]	M_A_PARITY_N	<<	>>
[13]	M_A_ALERT_N	<<	>>

[14]	M_DATA[0..63]	<<>>
[14]	M_B_DQS_DN0[7]	<<>>
[14]	M_B_DQS_DP0[7]	<<>>
[14]	M_B_A0[13]	<<>>
[14]	M_B_B00	<<>>
[14]	M_B_B01	<<>>
[14]	M_B_A17	<<>>
[14]	M_B_DM0[0..7]	<<>>
[14]	M_B_CKE0	<<>>
[14]	M_B_CKE1	<<>>
[14]	M_B_CS0_N	<<>>
[14]	M_B_CS1_N	<<>>
[14]	M_B_ODT0	<<>>
[14]	M_B_ODT1	<<>>
[14]	M_B_BA0	<<>>
[14]	M_B_BA1	<<>>
[14]	M_B_CLK0_P	<<>>
[14]	M_B_CLK0_N	<<>>
[14]	M_B_CLK1_P	<<>>
[14]	M_B_CLK1_N	<<>>
[14]	M_B_DRAMRST_N	<<>>
[14]	M_B_A14_WE_N	<<>>
[14]	M_B_A15_CAS_N	<<>>
[14]	M_B_A16_RAS_N	<<>>
[14]	M_B_ACT_N	<<>>
[14]	M_B_EVENT_N	<<>>
[14]	M_B_PARITY	<<>>
[14]	M_B_ALERT_N	<<>>

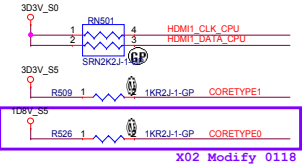


[56]	HDMI1_DATA_LS_P0	>>
[56]	HDMI1_DATA_LS_N0	>>
[56]	HDMI1_DATA_LS_P1	>>
[56]	HDMI1_DATA_LS_N1	>>
[56]	HDMI1_DATA_LS_P2	>>
[56]	HDMI1_DATA_LS_N2	>>
[56]	HDMI1_DATA_LS_P3	>>
[56]	HDMI1_DATA_LS_N3	>>
[56]	HDMI1_DATA_CPU	>>
[56]	HDMI1_CLK_CPU	>>
[6,56]	HDMI1_HPD	>>

X03_0209_ModiFy



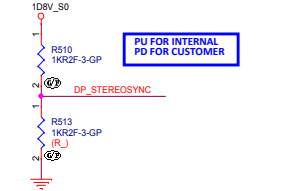
[99]	APU_TCK		
[99]	APU_TDI		
[99]	APU_TDO		
[99]	APU_TMS		
[99]	APU_TRST_N		
[99]	APU_DBDY		
[99]	APU_DBREQ_N		
[99]	APU_TEST18		
[99]	APU_TEST19		
[46,99]	APU_PWROK		
[99]	APU_RST_N		



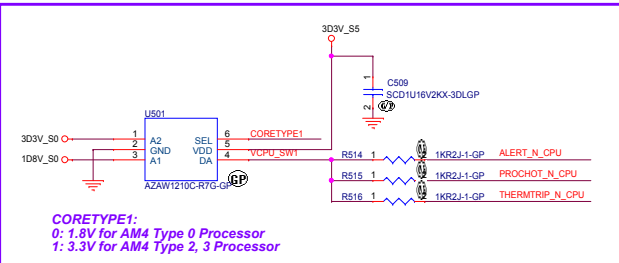
[46] SVID_CLK <<—

[46] SVID_DATA <<—

[46] SVID_SVT <<—

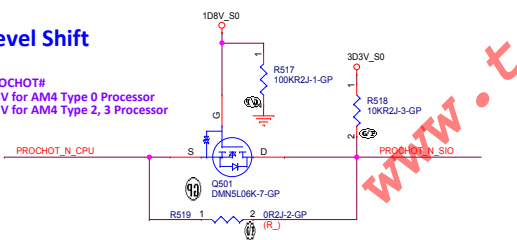
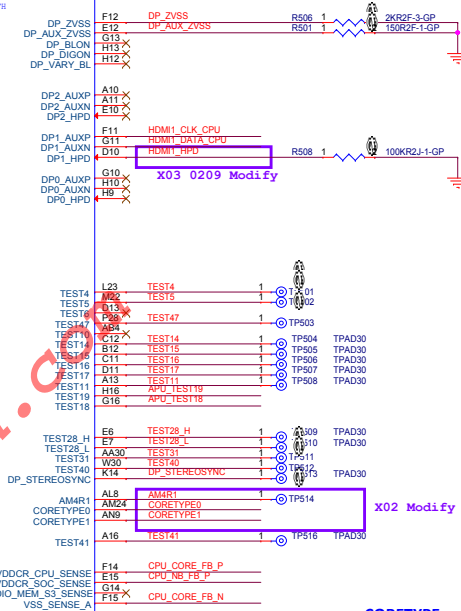
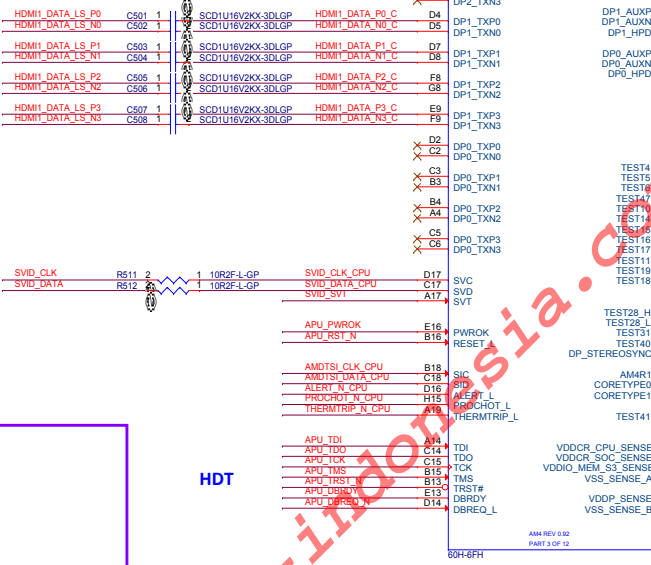


[24] AMDTSI_DATA_SIO << >>—
[24] AMDTSI_CLK_SIO >>—
[24,46] PROCHOT_N_SIO <<—



```
[46] CPU_NB_FB_P <<-----
[46] CPU_CORE_FB_P <<-----
[46] CPU_CORE_FB_N <<-----
[34,49,91] CORETYPE1 <<-----
[25] CORETYPE0 <<-----
X02 Modify 0118
```

PROCHOT#
1.8V for AM4 Type 0 Processor
3.3V for AM4 Type 2, 3 Processor

[illegible]

CORETYPE1	COPETYPE0	AM4 Processor Type
0	0	Type0
0	1	Reserved
1	0	Type2
1	1	Type3

AUDIO CODIC

[27] HDA_SDIN0_CPU
[27] HDA_RST_N_CPU
[27] HDA_SYNC_CODECC
[27] HDA_SDOOUT_CODECC
[27] HDA_BITCLK_CODECC

SM BUS

[13,14,64] SMB_DATA_MAIN
[13,14,64] SMB_CLK_MAIN
[71,93,94,95] SMB_CLK_RESUME
[71,93,94,95] SMB_DATA_RESUME

M.2 WLAN

[61] W1_DISABLE_N
[61] W2_DISABLE_N
[61] WLAN_PEDET

SIO

[24] PM_PWRBTN_N
[24,68] LPC_RST_N
[18] LPC_SMI_N
[18,24] LPC_PME_N

MISC

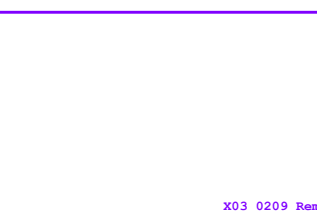
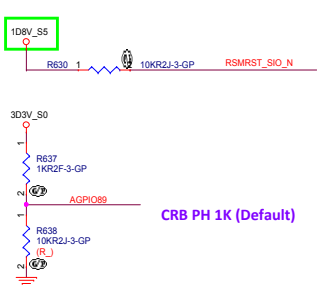
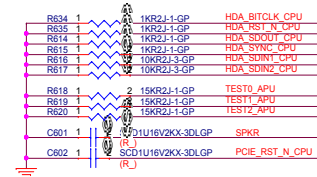
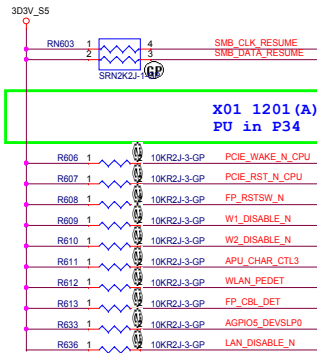
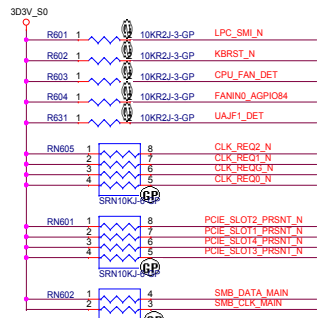
[18,31,36,61,62,93,94,95] PCIE_WAKE_N
[18,31,91,93,95] PCIE_RST_N_CPU
[12] FP_RSTSW_N
[24,32,33,34,38,39,45,50,71] SLP_S5_N
[24,38,41,42,50] S5_MUX_APU
[12] RTC_CLK_CPU
[24] RSMRST_SIO_N
[40] ALL_SYS_PWRGD
[93] CLK_REQ0_N
[93] CLK_REQ1_N
[31] CLK_REQ2_N
[12] AGPIO3_APU
[27] SPKR
[24] KBRST_N

GPIO

[7,25] PW_CLEAR
[64] FP_CBL_DET
[93] PCIE_SLOT1_PSRNT_N
[95] PCIE_SLOT2_PSRNT_N
[95] PCIE_SLOT3_PSRNT_N
[94] PCIE_SLOT4_PSRNT_N
[26] CPU_FAN_DET
[71] TYPEC_INT
[71] TYPEC_WP
[38] APU_CHAR_CTL3
[25] FDT_OVRD_GPIO
[30] UAFI_DET
[31] LAN_DISABLE_N
[5,56] HDMI1_HPD
X03 0209 HDMI detect

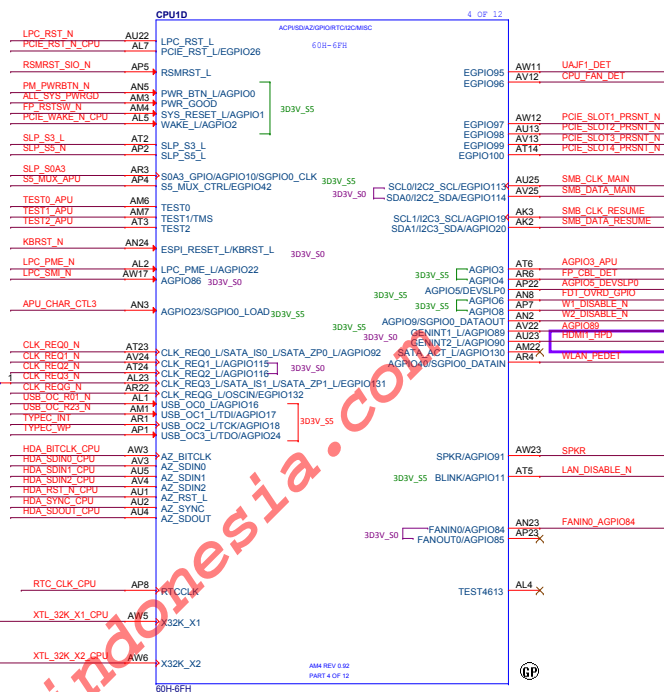
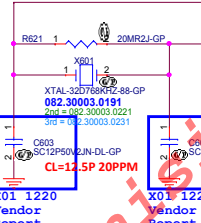
USB OC

[34] USB_OC_R01_N
[34] USB_OC_R23_N



X01 1201 (A)
PU in P34

XTAL 32.768KHz



CPU1G 7 OF 12

GND 60H-6FH

J15	VSS_397	VSS_60	E35
L29	VSS_398	VSS_61	E38
AJ11	VSS_399	VSS_62	F1
A3	VSS_1	VSS_63	F4
A6	VSS_2	VSS_64	F17
A9	VSS_3	VSS_65	F19
A12	VSS_4	VSS_66	F22
A15	VSS_5	VSS_67	F25
A18	VSS_6	VSS_68	F28
A21	VSS_7	VSS_69	F31
A24	VSS_8	VSS_70	F34
A27	VSS_9	VSS_71	F35
A30	VSS_10	VSS_72	F37
A33	VSS_11	VSS_73	G7
A36	VSS_12	VSS_74	G21
B19	VSS_13	VSS_75	G24
B23	VSS_14	VSS_76	G27
B26	VSS_15	VSS_77	G30
B29	VSS_16	VSS_78	G33
B32	VSS_17	VSS_79	G35
B35	VSS_18	VSS_80	G36
C1	VSS_19	VSS_81	G39
C22	VSS_20	VSS_82	H4
C25	VSS_21	VSS_83	H5
C28	VSS_22	VSS_84	H8
C31	VSS_23	VSS_85	H11
C34	VSS_24	VSS_86	H14
C37	VSS_25	VSS_87	H17
D6	VSS_26	VSS_88	H20
D9	VSS_27	VSS_89	H23
D12	VSS_28	VSS_90	H26
D15	VSS_29	VSS_91	H29
D18	VSS_30	VSS_92	H32
D19	VSS_31	VSS_93	H35
D21	VSS_32	VSS_94	H38
D22	VSS_33	VSS_95	J1
D23	VSS_34	VSS_96	J4
D24	VSS_35	VSS_97	J8
D25	VSS_36	VSS_98	J9
D27	VSS_37	VSS_99	J11
D29	VSS_38	VSS_100	J13
D30	VSS_39	VSS_101	J17
D31	VSS_40	VSS_102	J19
D32	VSS_41	VSS_103	J22
D33	VSS_42	VSS_104	J25
D34	VSS_43	VSS_105	J28
D35	VSS_44	VSS_106	J31
D36	VSS_45	VSS_107	J34
D39	VSS_46	VSS_108	J35
E4	VSS_47	VSS_109	J37
E5	VSS_48	VSS_110	K10
E8	VSS_49	VSS_111	K12
E11	VSS_50	VSS_112	K18
E14	VSS_51	VSS_113	K20
E17	VSS_52	VSS_114	K21
E20	VSS_53	VSS_115	K22
E21	VSS_54	VSS_116	K23
E23	VSS_55	VSS_117	K26
E26	VSS_56	VSS_118	K27
E27	VSS_57	VSS_119	K28
E29	VSS_58	VSS_120	K29
E32	VSS_59	VSS_121	K30

AM4 REV 0.02
PART 7 OF 12

60H-6FH



CPU1H 8 OF 12

GND 60H-6FH

K33	VSS_122	VSS_184	U13
L4	VSS_123	VSS_185	U27
L5	VSS_124	VSS_186	U29
L8	VSS_125	VSS_187	U31
L9	VSS_126	VSS_188	V1
L11	VSS_127	VSS_189	V4
L13	VSS_128	VSS_190	V7
L15	VSS_129	VSS_191	V10
L17	VSS_130	VSS_192	V12
L19	VSS_131	VSS_193	V20
L21	VSS_132	VSS_194	V30
L25	VSS_133	VSS_195	W9
L27	VSS_134	VSS_196	W11
L28	VSS_135	VSS_197	W13
L30	VSS_136	VSS_198	W27
L31	VSS_137	VSS_199	W29
M1	VSS_138	VSS_200	W31
M4	VSS_139	VSS_201	Y5
M8	VSS_140	VSS_202	Y8
M10	VSS_141	VSS_203	Y10
M12	VSS_142	VSS_204	Y12
M14	VSS_143	VSS_205	Y28
M16	VSS_144	VSS_206	Y30
M18	VSS_145	VSS_207	AA1
M20	VSS_146	VSS_208	AA4
M24	VSS_147	VSS_209	AA6
M26	VSS_148	VSS_210	AA9
M28	VSS_149	VSS_211	AA11
N9	VSS_150	VSS_212	AA13
N11	VSS_151	VSS_213	AA27
N13	VSS_152	VSS_215	AA31
N15	VSS_153	VSS_214	AA29
N17	VSS_154	VSS_216	AB7
N19	VSS_155	VSS_217	AB10
N21	VSS_156	VSS_218	AB12
N23	VSS_157	VSS_219	AB17
N25	VSS_158	VSS_220	AB28
N27	VSS_159	VSS_221	AB30
N29	VSS_160	VSS_222	AC5
P4	VSS_161	VSS_223	AC8
P5	VSS_162	VSS_224	AC9
P8	VSS_163	VSS_225	AC11
P10	VSS_164	VSS_226	AC13
P12	VSS_165	VSS_227	AC27
P13	VSS_166	VSS_228	AC29
R1	VSS_167	VSS_229	AC31
R4	VSS_168	VSS_230	AD1
R9	VSS_169	VSS_231	AD4
R11	VSS_170	VSS_232	AD10
R13	VSS_171	VSS_233	AD12
R27	VSS_172	VSS_234	AD28
R29	VSS_173	VSS_235	AD30
T10	VSS_174	VSS_236	AE7
T12	VSS_175	VSS_237	AE9
T28	VSS_176	VSS_238	AE11
T30	VSS_177	VSS_239	AE13
U4	VSS_178	VSS_240	AE27
U5	VSS_179	VSS_241	AE29
U8	VSS_180	VSS_242	AE31
U9	VSS_181	VSS_243	AF5
U11	VSS_182	VSS_244	AF8
	VSS_183	VSS_245	AF10
			AF12

AM4 REV 0.02
PART 8 OF 12

60H-6FH



CPU1J 10 OF 12

GND 60H-6FH

AF28	VSS_246	VSS_308	AL30
AF30	VSS_247	VSS_309	AL33
AG1	VSS_248	VSS_310	AL35
AG4	VSS_249	VSS_311	AL36
AG8	VSS_250	VSS_312	AL39
AG9	VSS_251	VSS_313	AM5
AG11	VSS_252	VSS_314	AM11
AG13	VSS_253	VSS_315	AM14
AG15	VSS_254	VSS_316	AM26
AG17	VSS_255	VSS_317	AM29
AG19	VSS_256	VSS_318	AM32
AG21	VSS_257	VSS_319	AM35
AG23	VSS_258	VSS_320	AN1
AG25	VSS_259	VSS_321	AN4
AG27	VSS_260	VSS_322	AN22
AG28	VSS_261	VSS_323	AN25
AG29	VSS_262	VSS_324	AN28
AG30	VSS_263	VSS_325	AN31
AG31	VSS_264	VSS_326	AN34
AG32	VSS_265	VSS_327	AN35
AH10	VSS_266	VSS_328	AN37
AH12	VSS_267	VSS_329	AP6
AH16	VSS_268	VSS_330	AP24
AH18	VSS_269	VSS_331	AP27
AH20	VSS_270	VSS_332	AP30
AH22	VSS_271	VSS_333	AP33
AH24	VSS_272	VSS_334	AP35
AH26	VSS_273	VSS_335	AP36
AH28	VSS_274	VSS_336	AP39
AH29	VSS_275	VSS_337	AR5
AH30	VSS_276	VSS_338	AR8
AH33	VSS_277	VSS_339	AR11
AJ5	VSS_278	VSS_340	AR14
AJ8	VSS_279	VSS_341	AR26
AJ9	VSS_280	VSS_342	AR23
AJ13	VSS_281	VSS_343	AR26
AJ23	VSS_282	VSS_344	AR27
AJ25	VSS_283	VSS_345	AR29
AJ26	VSS_284	VSS_346	AR30
AJ27	VSS_285	VSS_347	AR32
AJ28	VSS_286	VSS_348	AR34
AJ29	VSS_287	VSS_349	AR35
AJ32	VSS_288	VSS_350	AR38
AJ35	VSS_289	VSS_351	AT1
AJ36	VSS_290	VSS_352	AT7
AJ38	VSS_291	VSS_353	AT10
AK1	VSS_292	VSS_354	AT13
AK4	VSS_293	VSS_355	AT16
AK10	VSS_294	VSS_356	AT22
AK12	VSS_295	VSS_357	AT26
AK14	VSS_296	VSS_358	AT27
AK22	VSS_297	VSS_359	AT28
AK25	VSS_298	VSS_360	AT29
AK28	VSS_299	VSS_361	AT31
AK31	VSS_300	VSS_362	AT32
AK35	VSS_301	VSS_363	AT33
AK37	VSS_302	VSS_364	AT34
AL9	VSS_303	VSS_365	AT37
AL11	VSS_304	VSS_366	AU18
AL24	VSS_305	VSS_367	AU21
AL27	VSS_306	VSS_368	AU24
	VSS_307	VSS_369	

AM4 REV 0.02
PART 10 OF 12

60H-6FH



CPU1K 11 OF 12

GND & RSVD-6FH

AU26	VSS_370	RSVD_24	AM12
AU27	VSS_371	RSVD_45	AT28
AU30	VSS_372	RSVD_37	AR15
AU33	VSS_373	RSVD_33	AP15
AU36	VSS_374	RSVD_28	AN12
AU39	VSS_375	RSVD_29	AN15
AV2	VSS_376	RSVD_46	AT30
AV17	VSS_377	RSVD_47	AW24
AV20	VSS_378	RSVD_43	AR24
AV23	VSS_379	RSVD_40	AS
AV26	VSS_380	RSVD_14	AD3
AV29	VSS_381	RSVD_12	AB2
AV32	VSS_382	RSVD_15	AH2
AV35	VSS_383	RSVD_18	AL16
AV38	VSS_384	RSVD_19	AL17
AW4	VSS_385	RSVD_20	AL18
AW7	VSS_386	RSVD_21	AL19
AW10	VSS_387	RSVD_22	AL20
AW13	VSS_388	RSVD_23	AL21
AW16	VSS_389	RSVD_25	AM16
AW19	VSS_390	RSVD_26	AM17
AW22	VSS_391	RSVD_27	AM21
AW25	VSS_392	RSVD_30	AN16
AW28	VSS_393	RSVD_31	AN17
AW31	VSS_394	RSVD_32	AN21
AW34	VSS_395	RSVD_34	AP16
AW37	VSS_396	RSVD_35	AP17
		RSVD_36	AP21
		RSVD_38	AR16
		RSVD_39	AR18
		RSVD_40	AR19
		RSVD_41	AR20
		RSVD_42	AR21
		RSVD_44	AT18
		RSVD_2	D28
		RSVD_3	E19
		RSVD_4	E22
		RSVD_5	E25
		RSVD_6	G17
		RSVD_7	J36
		RSVD_8	J38
		RSVD_9	K34
		RSVD_10	K38
		RSVD_11	R35
		RSVD_13	AB37
		RSVD_16	AH35
		RSVD_17	AK34

AM4 REV 0.02
PART 11 OF 12

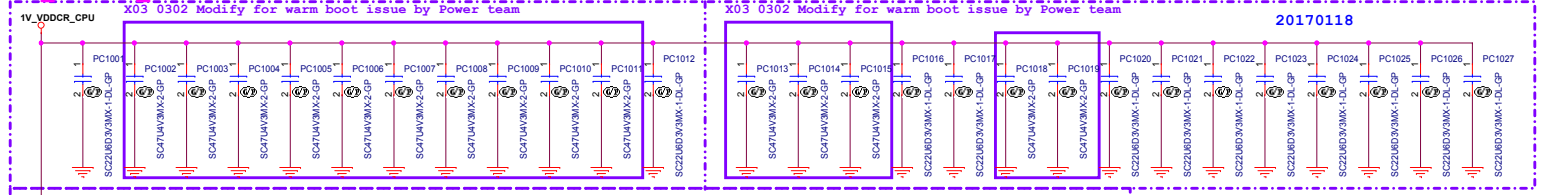
60H-6FH



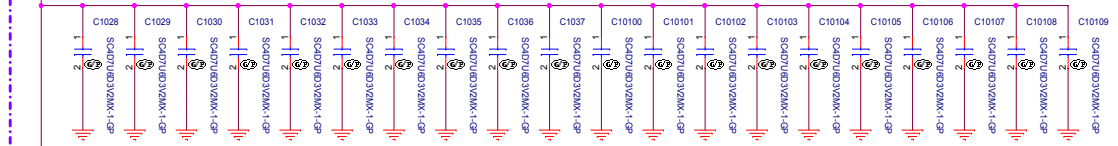
1V VDDCR_CPU

CRB/Checklist: 22uF*27 4.7uF*20 0.22uF*12 180pF*2

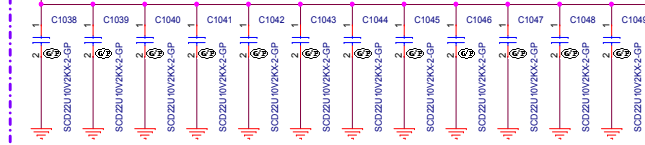
Bottom Side: 22uF 0603 x15 sets



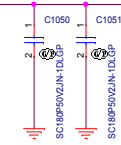
Bottom Side: 4.7uF 0402 x20 sets



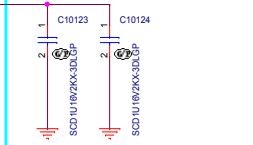
Bottom Side: 0.22uF 0402 x12 sets



180pF 0402 x2 sets



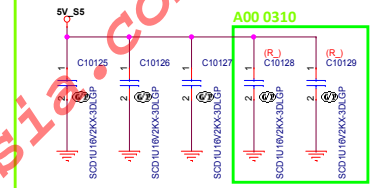
Moat Cap 0.1uF 0402 *2 sets



X00 1026

A00 0308

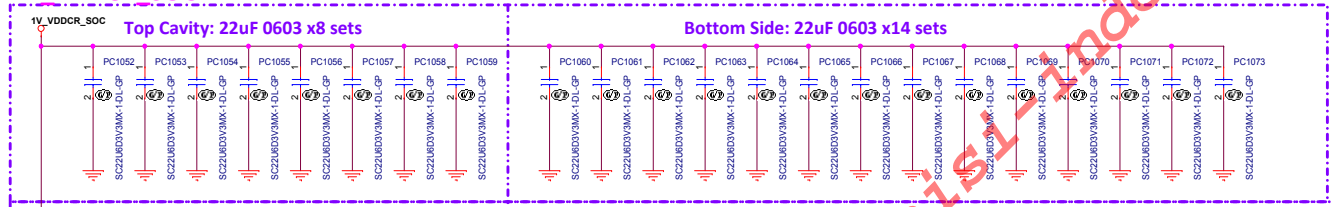
Moat Cap 0.1uF 0402 *3 sets



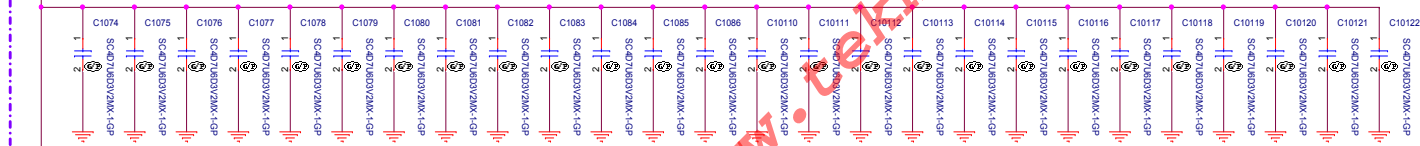
1V VDDCR_SOC

CRB/Checklist: 22uF*22 4.7uF*26 0.22uF*10 180pF*3

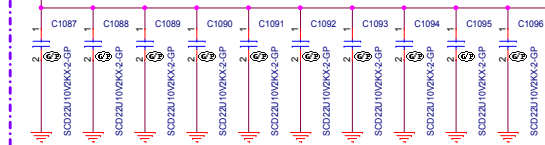
X01 1216 for power team



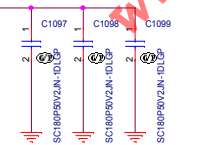
Bottom Side: 4.7uF 0402 x26 sets



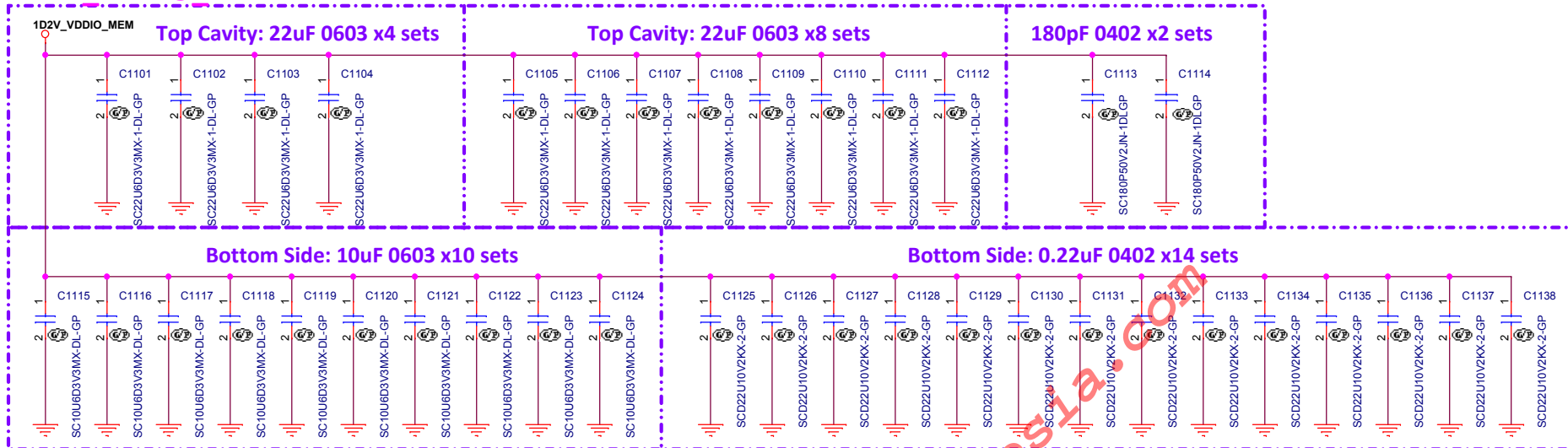
Bottom Side: 0.22uF 0402 x10 sets



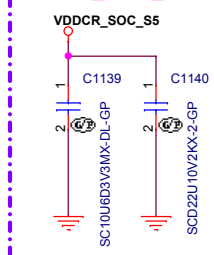
180pF 0402 x3 sets



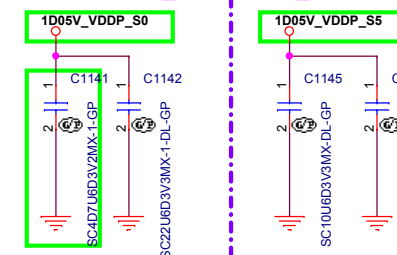
1D2V_VDDIO_MEM



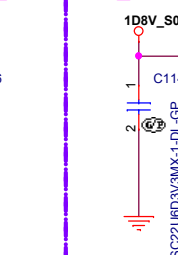
VDDCR_SOC_S5



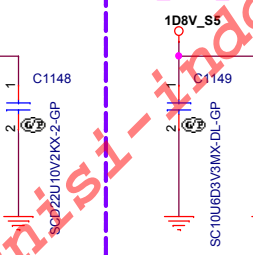
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VDDP_S5(1D05V_S5)_VDD_1D8



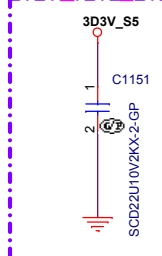
VDD_1D8_S5



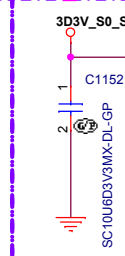
VDD_1D8_S5



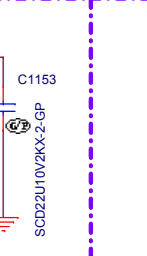
VDD_3D3_S5



VDD_3D3



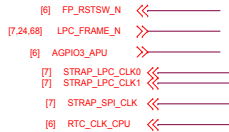
VDDIO_AUDIO



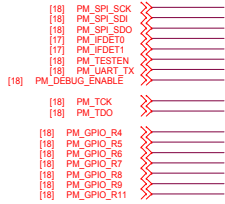
1D5V_VDDBT_RTC



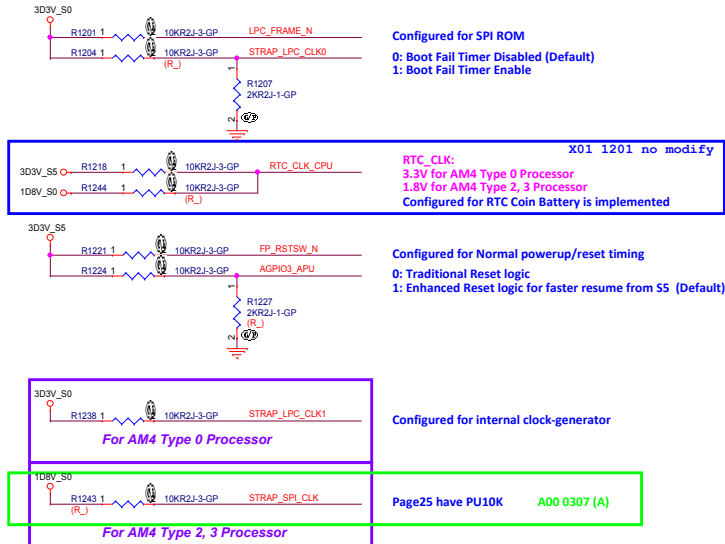
APU



PROM



AM4 APU HW Strap

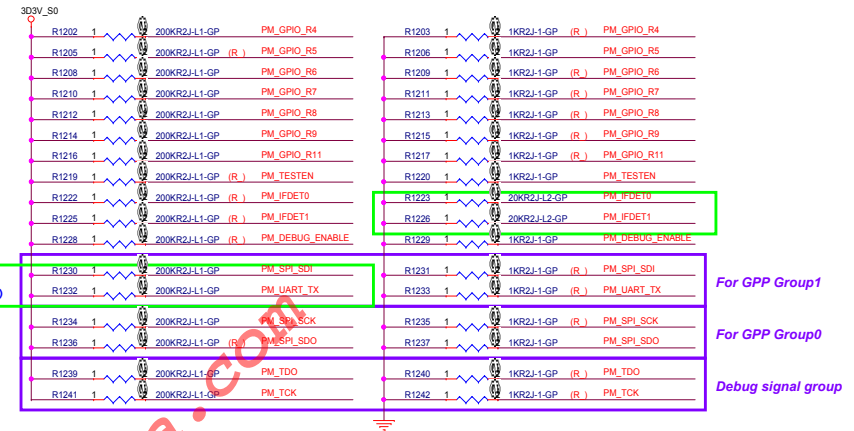


Strap Name	Signal Name	Strap Type	Default Value	Bit Value	Description
CLKGEN AM4 Type 0, Type 2, and Type 3 processors	LPCCCLK1	Strap II	1	0	Reserved
	SPI_CLK			1	Configured for internal clock-generator LPCCCLK1 = 10 kΩ (± 5%) pull-up resistor to VDD_33 SPI_CLK = 10 kΩ (± 5%) pull-up resistor to VDD_18
ShortReset AM4 Type 0, Type 2, and Type 3 processors	SYS_RESET_L	Strap I	1	0	Reserved
				1	Normal powerup/reset timing 10 kΩ (± 5%) pull-up resistor to VDD_33_S5
ROMTYPE AM4 Type 0 and Type 2 processors only	LFRAME_L	Strap II	1	0	LPC ROM
				1	SPI ROM 10 kΩ (± 5%) pull-up resistor to VDD_33
BOOTFAILTIMER AM4 Type 0 processor only	LPCCLK0	Strap II	0	0	Boot Fail Timer Disabled
				1	Boot Fail Timer Enabled 10 kΩ (± 5%) pull-up resistor to VDD_33
RTC Coin Battery AM4 Type 0 processor only	RTCCLK	Strap I	1	0	RTC Coin Battery is not implemented
				1	RTC Coin Battery is implemented 10 kΩ (± 5%) pull-up resistor to VDD_33_S5
Alternate Reset AM4 Type 0 processor only	AGPIO3	Strap I	1	0	Traditional Reset logic
				1	Enhanced Reset logic for faster resume from S5 10 kΩ (± 5%) pull-up resistor to VDD_33_S5

Note:

- To ensure Alternate Reset strap can capture correct information, platform has to make sure AGPIO3 has valid voltage config. value until 20 ms after RSMRST_L has risen to at least 3.0 v.
- AGPIO3 can be used as a GPIO as long as the signal is not driven on during S5 to S0 (during Resume reset time).

PROMONTORY HW Strap



Strapping Pins	Function
TESTEN	Test mode enable 1: Test mode 0: Function mode
IFDET1	SATA Express port1 1: PCIe mode; 0: SATA mode
IFDET0	SATA Express port0 1: PCIe mode; 0: SATA mode
DEBUG_ENABLE	1: Debug mode 0: Function mode
TCK (DEBUG_SEL1) TDO (DEBUG_SELO)	11: Debug signal group 3 output 10: Debug signal group 2 output 01: Debug signal group 1 output 00: Debug signal group 0 output
UART_TX (GPP_G1_SET1)	GPP Group1 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved
SPI_SDI (GPP_G1_SET0)	GPP Group0 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved
SPI_SDO (GPP_G0_SET1)	GPP Group0 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved
SPI_SCK (GPP_G0_SET0)	GPP Group0 11: 1 PCIe x4; 10: 1 PCIe x2+2 PCIe x1; 01: 4 PCIe x1; 00: Reserved
GPIO_R4	1: GPP clock source from APU_CLKP/N; 0: GPP clock source from Crystal, also enables GPIO_R8
GPIO_R5	1: USBCC SSC disable 0: USBCC SSC enable
GPIO_R6	1: SATA SSC disable 0: SATA SSC enable
GPIO_R7	1: SATA Express SSC disable 0: SATA Express SSC enable
GPIO_R8	1: GPP SSC disable 0: GPP SSC enable
GPIO_R11	1: GPP clock output enabled 0: GPP clock output disabled

[4] M_DATA_B[0..63] <<>>>>
[4] M_B_DM[0..7] <<>>>>

[4] M_B_DQS_DN[0..7] <<>>>>
[4] M_B_DQS_DP[0..7] <<>>>>

[4] M_B_A[0..13] << >>

[4] M_B_A17 << >>

[4] M_B_A14_WE_N << >>

[4] M_B_A15_CAS_N << >>

[4] M_B_A16_RAS_N << >>

[4] M_B_BA0 << >>

[4] M_B_BA1 << >>

[4] M_B_BG0 << >>

[4] M_B_BG1 << >>

[4] M_B_CS0_N
[4] M_B_CS1_N
[4] M_B_CKE0
[4] M_B_CKE1
[4] M_B_ODT0
[4] M_B_ODT1

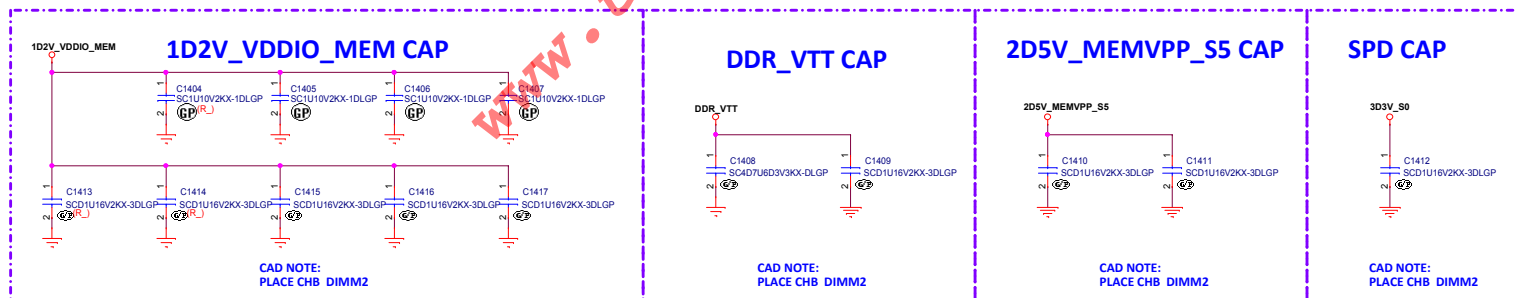
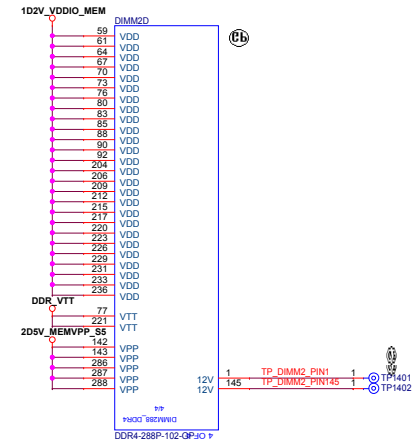
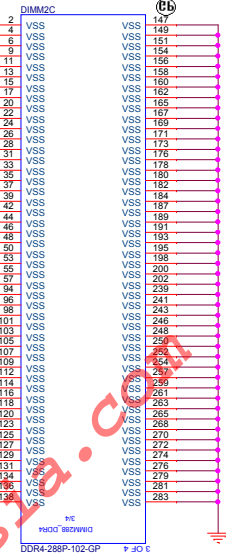
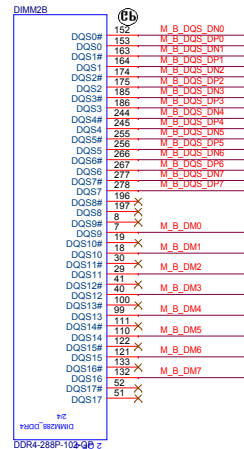
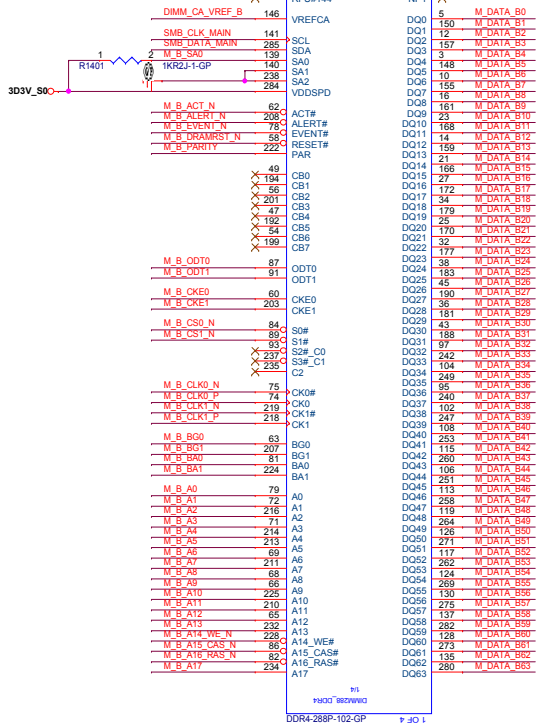
```

[4] M_B_CLK0_P
[4] M_B_CLK0_N
[4] M_B_CLK1_P
[4] M_B_CLK1_N

```

[6,13,64] SMB_DATA_MAIN
[6,13,64] SMB_CLK_MAIN

[4] M_B_DRAMRST_N
[4] M_B_EVENT_N
[4] M_B_PARITY
[4] M_B_ALERT_N
[4] M_B_ACT_N



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Document Number

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Rev

A00

Date: Friday, March 10, 2017

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Document Number

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Rev

A00

Date: Friday, March 10, 2017

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STRAP

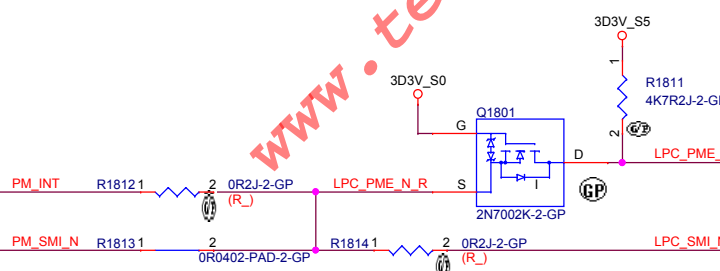
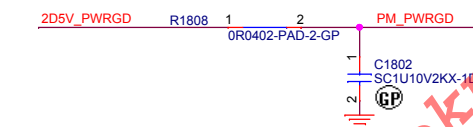
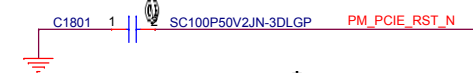
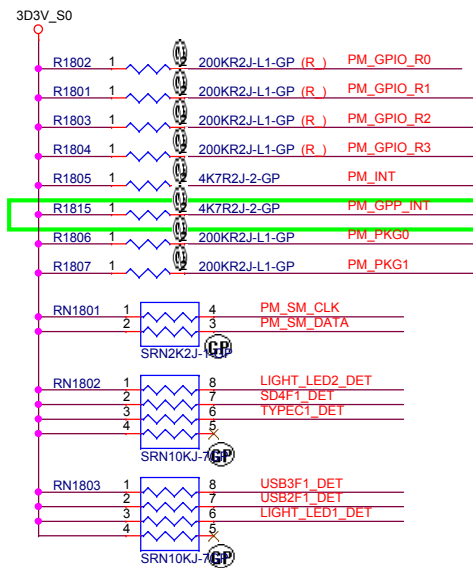
[12]	PM_SPI_SCK	<<-----
[12]	PM_SPI_SDI	<<-----
[12]	PM_SPI_SDO	<<-----
[12]	PM_TESTEN	<<-----
[12,18]	PM_UART_TX	<<-----
[12]	PM_TCK	<<-----
[12]	PM_TDO	<<-----
[12]	PM_DEBUG_ENABLE	<<-----
[12]	PM_GPIO_R4	<<-----
[12]	PM_GPIO_R5	<<-----
[12]	PM_GPIO_R6	<<-----
[12]	PM_GPIO_R7	<<-----
[12]	PM_GPIO_R8	<<-----
[12]	PM_GPIO_R9	<<-----
[12]	PM_GPIO_R11	<<-----

OTHER

[6]	LPC_SMI_N	<<-----
[6,24]	LPC_PME_N	<<-----
[46]	PM_PWRGD	<<-----
[45]	2D5V_PWRGD	>>-----
[6,31,36,61,62,93,94,95]	PCIE_WAKE_N	<<-----
[6,31,91,93,95]	PCIE_RST_N_CPU	<<-----
[36,61,62,94,95]	PM_PCIE_RST_N	<<-----
[12,18]	PM_UART_TX	<<-----

GPIO

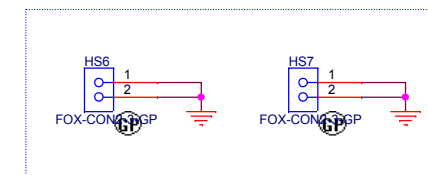
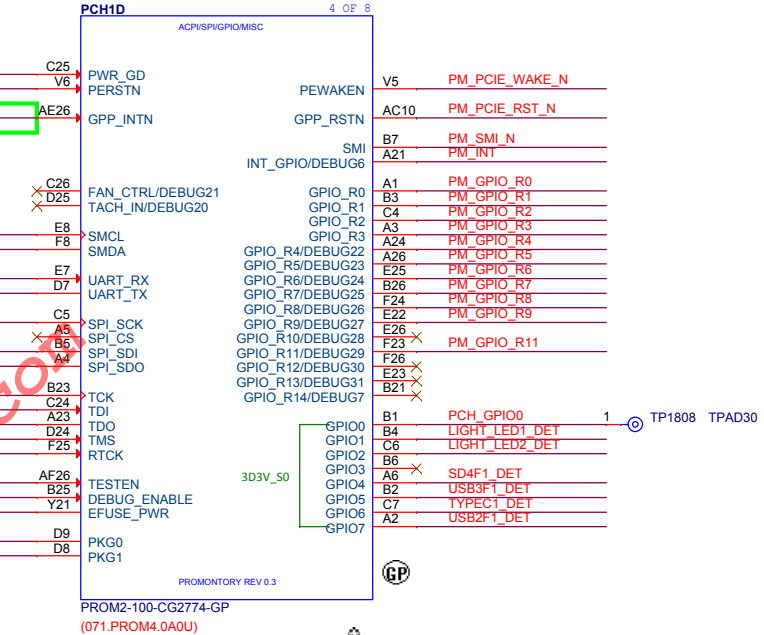
[64]	LIGHT_LED1_DET	>>-----
[64]	LIGHT_LED2_DET	>>-----
[36]	SD4F1_DET	>>-----
[37]	TYPEC1_DET	>>-----
[38]	USB3F1_DET	>>-----
[39]	USB2F1_DET	>>-----



X01 1201 (A)

X01 1201 (A)

2D5V_S0_PCH



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Title PROMONTORY_GPIO		
Size B	Document Number Red Skull	Rev A00
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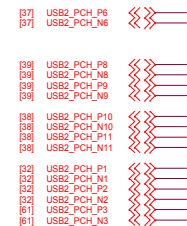
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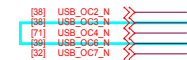
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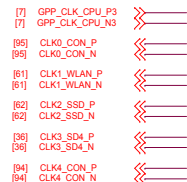
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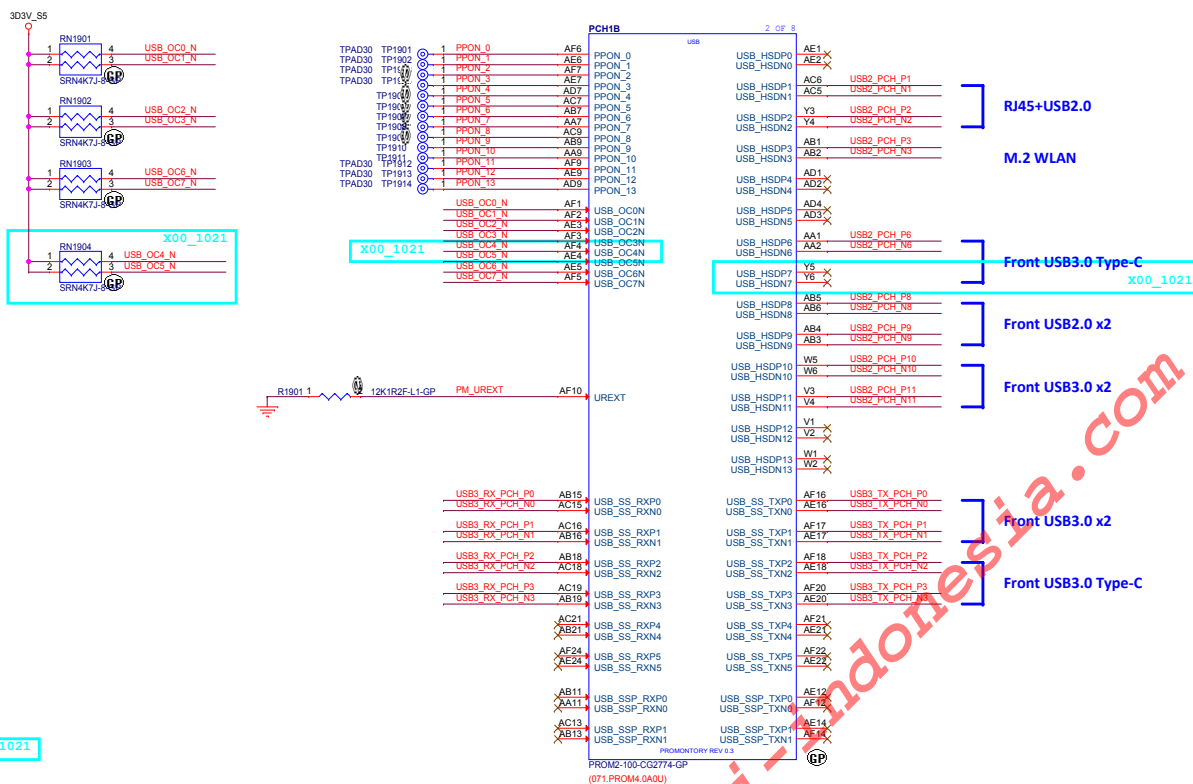
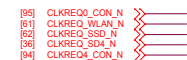
USB OC



CLOCK

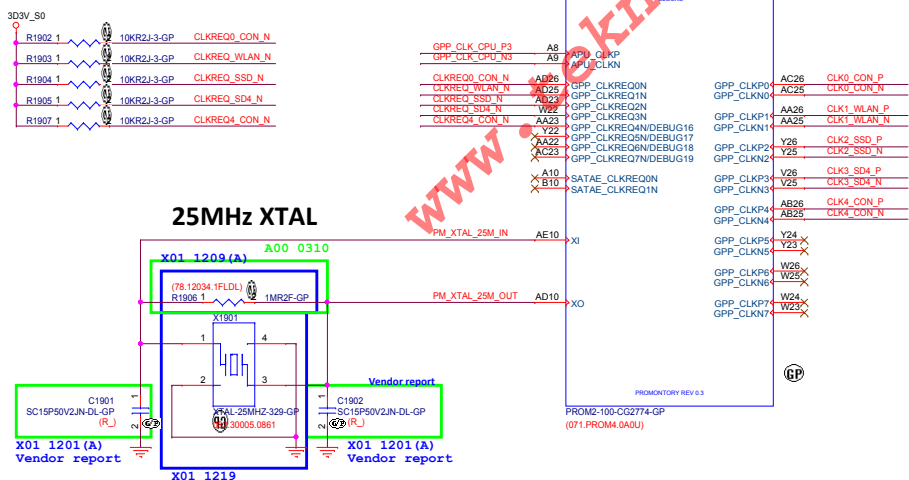


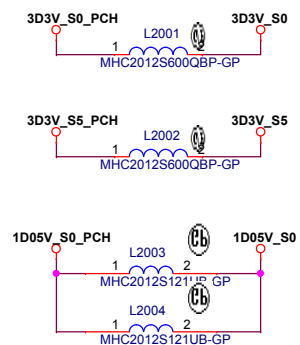
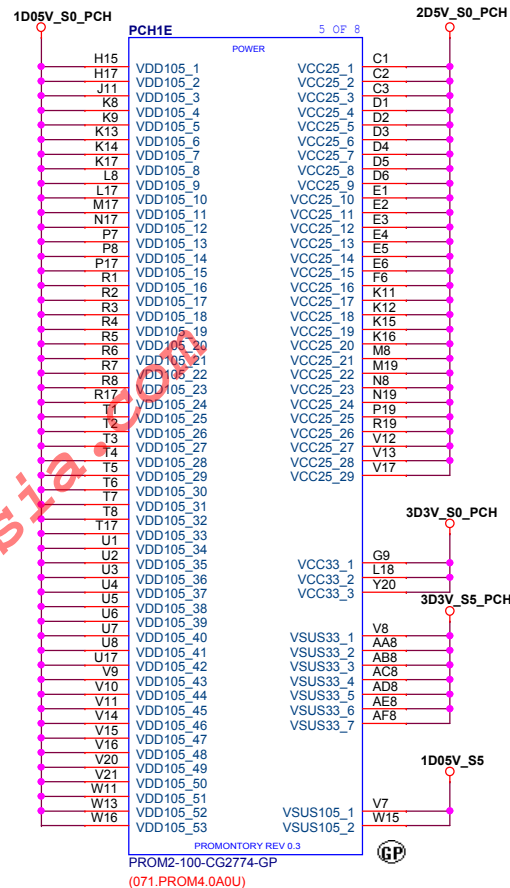
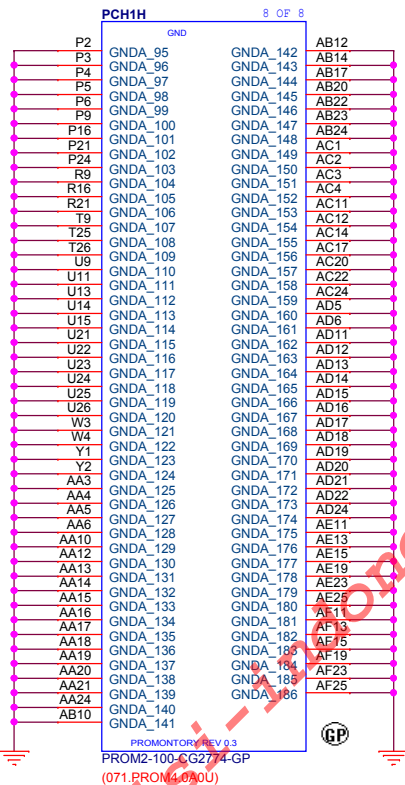
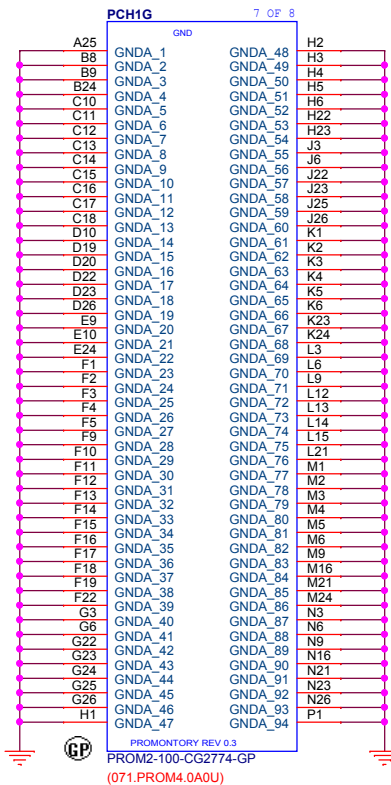
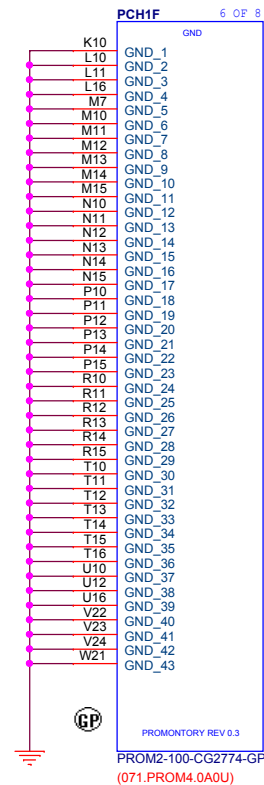
CLKREQ



Appendix D USB Port to OC Pin Mapping

USB3.1	USB2.0	USB_OC
USB_SSP_TX/RXP/N[0]	USB_HSDP/N[5]	USB_OC0N
USB_SSP_TX/RXP/N[1]	USB_HSDP/N[0]	USB_OC1N
USB3.0	USB2.0	USB_OC
USB_SS_TX/RXP/N[0]	USB_HSDP/N[10]	USB_OC2N
USB_SS_TX/RXP/N[1]	USB_HSDP/N[11]	USB_OC3N
USB_SS_TX/RXP/N[2]	USB_HSDP/N[6]	USB_OC4N
USB_SS_TX/RXP/N[3]	USB_HSDP/N[7]	USB_OC5N
USB_SS_TX/RXP/N[4]	USB_HSDP/N[8]	USB_OC6N
USB_SS_TX/RXP/N[5]	USB_HSDP/N[9]	USB_OC7N
	USB_HSDP/N[1]	USB_OC7N
	USB_HSDP/N[2]	USB_OC7N
	USB_HSDP/N[3]	USB_OC7N
	USB_HSDP/N[4]	USB_OC7N
	USB_HSDP/N[12]	USB_OC7N
	USB_HSDP/N[13]	USB_OC7N

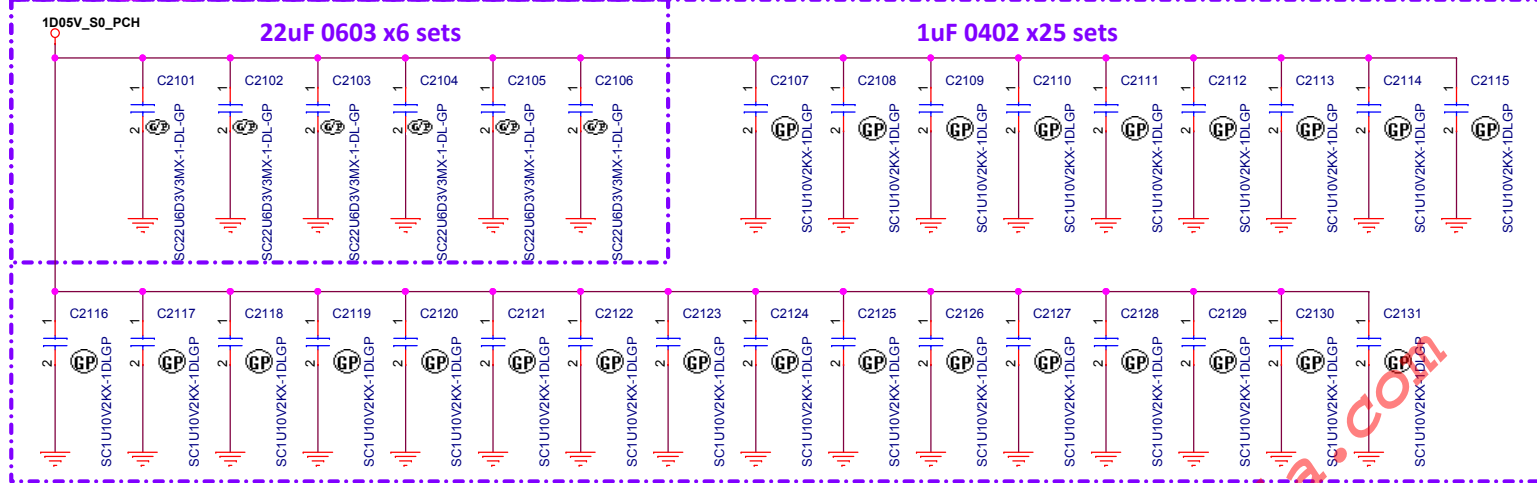




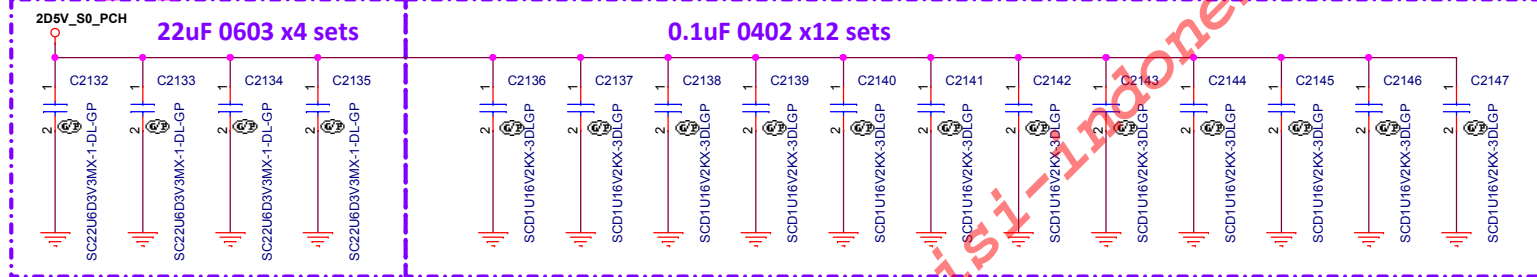
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Title PROMONTORY_Power		
Size B	Document Number Red Skull	Rev A00
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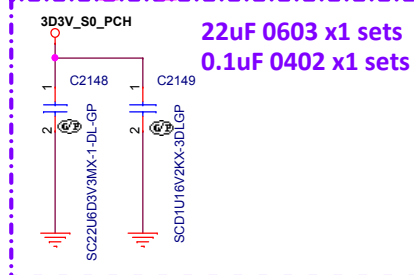
1D05V_S0_PCH



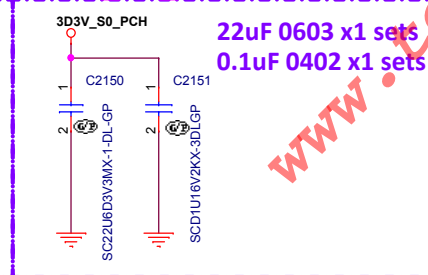
2D5V_S0_PCH



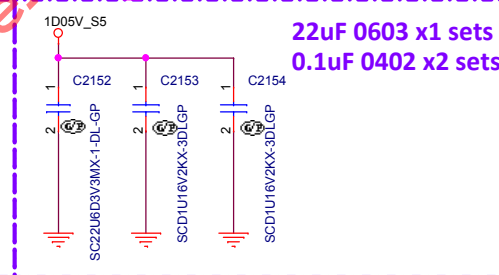
3D3V_S0_PCH



3D3V_S5_PCH



1D05V_S5



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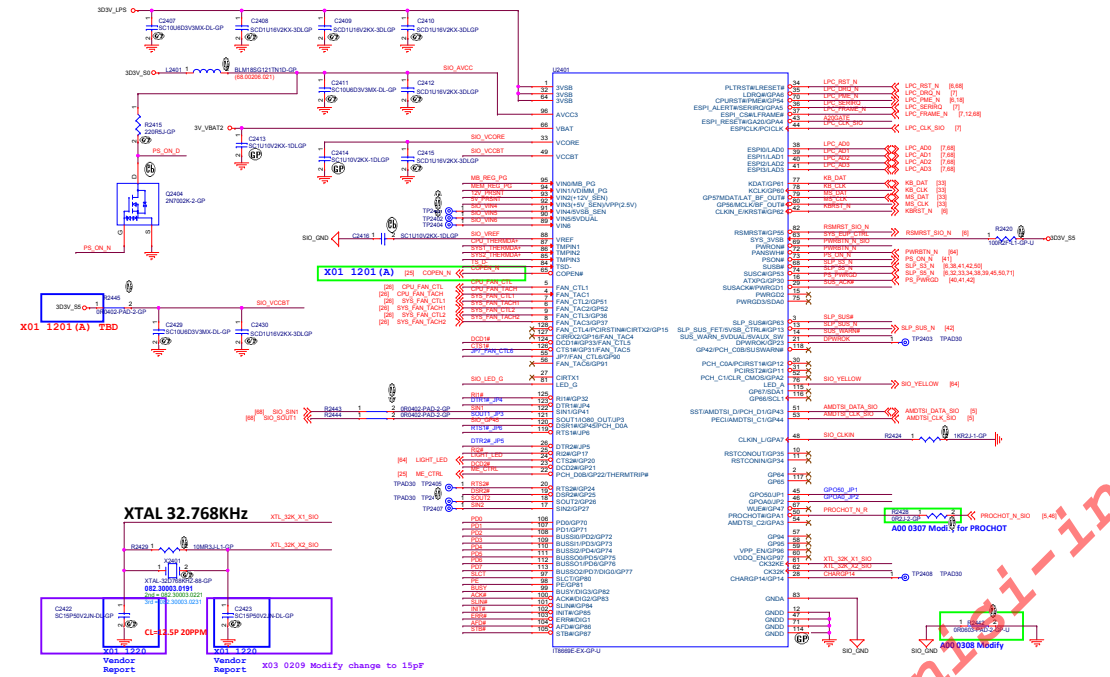
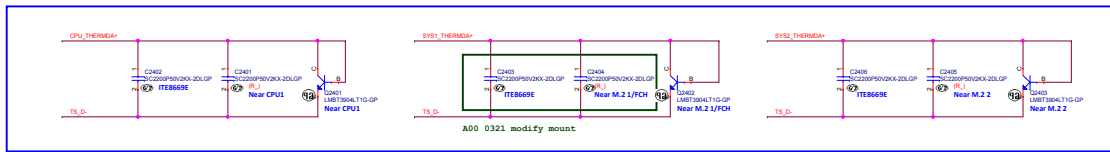
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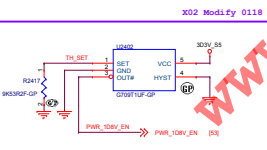


Thermal sensor G709

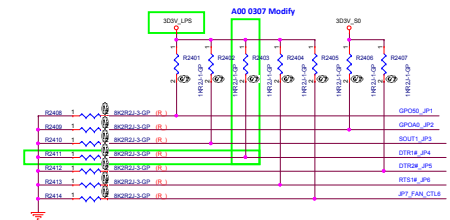
$$R_{SET} (K\Omega) = 0.0012T^2 - 0.9308T + 96.147$$

Temp. = 108 °C
RSET = 9.6174 Kohm

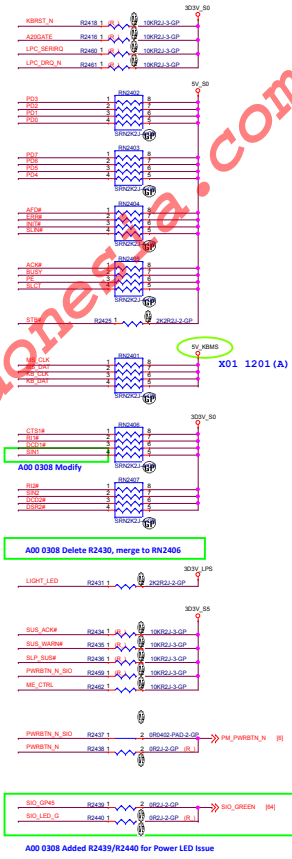
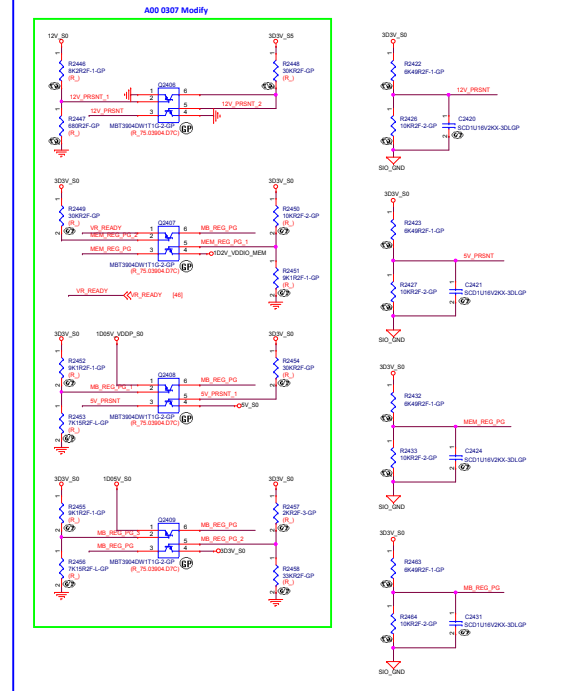
G709	
HYST = VCC	Hysteresis is 10°C
HYST = GND	Hysteresis is 2°C



SIO Power-On Strapping	Symbol	Value	Description
JP1	DSW_EUP_SEL	1	EUP
Pin-45	DSW	0	DSW
JP2	WDT_EN	1	Disable WDT to reset PWROK
Pin-46	WDT	0	Enable WDT to reset PWROK
JP3	VH/VIL_SEL	1	3.3V Level (Default)
Pin-121	VH/VIL	0	1.8V Level
JP4	DIAG_LED_SEL	1	Disable Diagnostic LED function
Pin-123	DIAG_LED	0	Enable Diagnostic LED function
JP5	UOVMODE_SEL	1	Notice Mode (Default)
Pin-26	OV/UV	0	Force Mode
JP6	LPC/eSPI	0	Enable LPC Interface
Pin-119	LPC	0	Enable eSPI Interface
JP7	DDR4_EN	1	Disable DDR4
Pin-55	DDR4	0	Enable DDR4



Circuit to Support pre-Post Diagnostic



SPI ROM

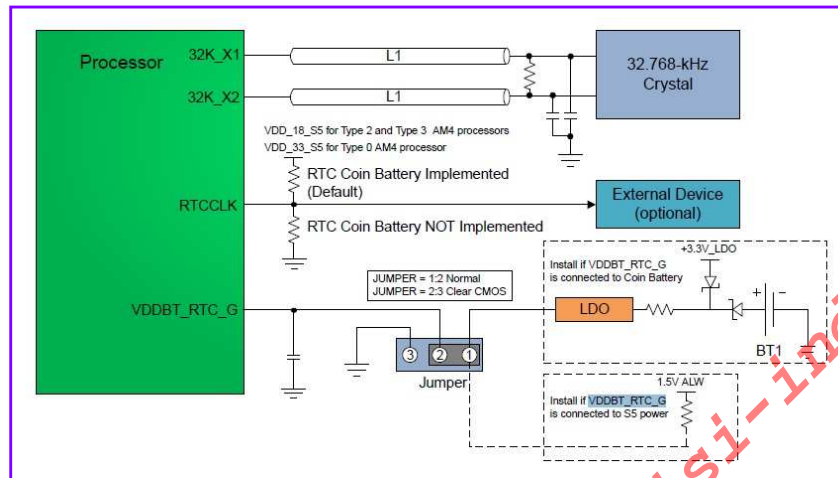
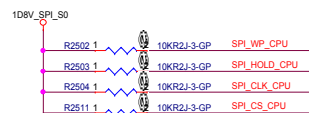
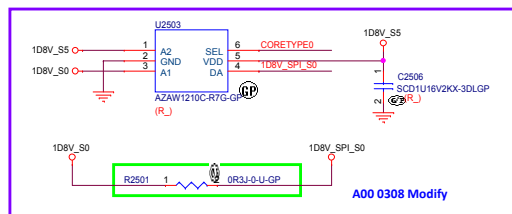
[7.91] SPI_SI_CPU <<
[7] SPI_HOLD_CPU <<
[7] SPI_WP_CPU <<
[7.91] SPI_SO_CPU <<
[7] SPI_CS_CPU <<
[7.91] SPI_CLK_CPU <<

JMP GPIO

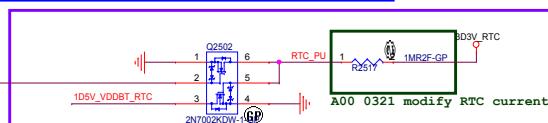
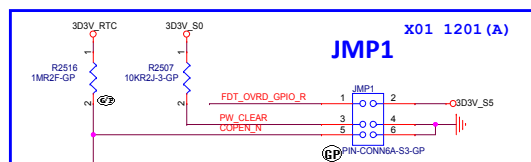
[24] ME_CTRL <<
[6] FDT_OVRD_GPIO <<
[7] PW_CLEAR <<
[24] COPEN_N <<

Other

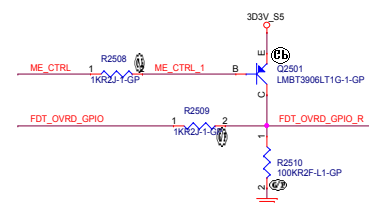
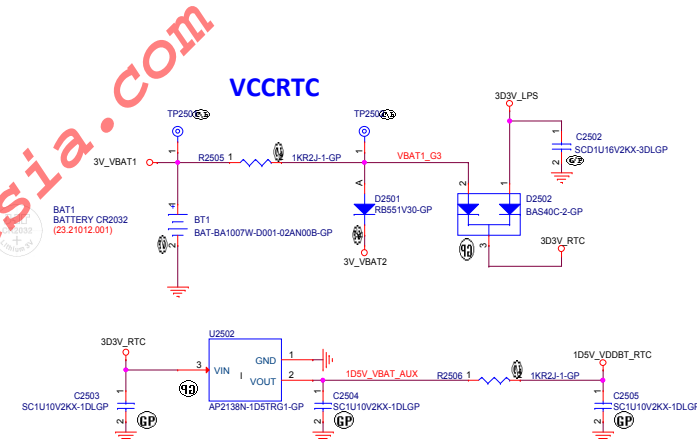
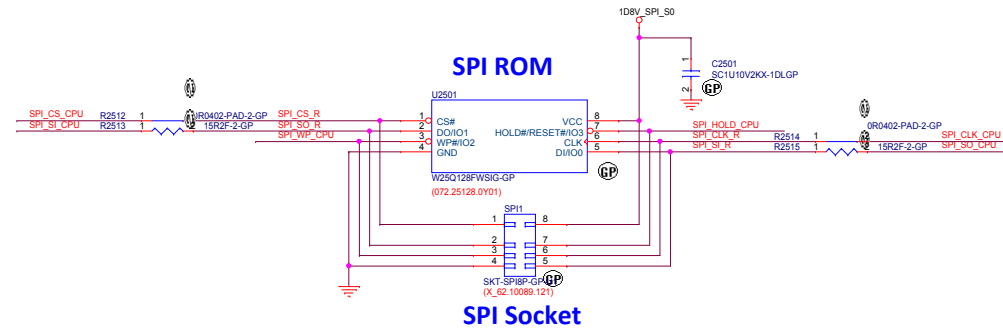
[5] CORETYPE0 <<
X02 Modify 0118



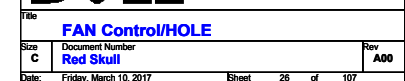
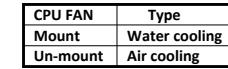
Jumper	Function	Operation
JMP1	SERVICE_MODE	1 - 2 SHORT : Disable
		1 - 2 OPEN : Default
	PASSWORD	3 - 4 SHORT : Default
		3 - 4 OPEN : Clear
	CMOS	5 - 6 SHORT : Clear
		5 - 6 OPEN : Default

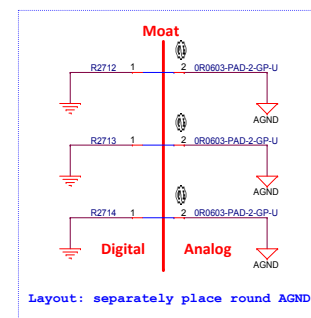
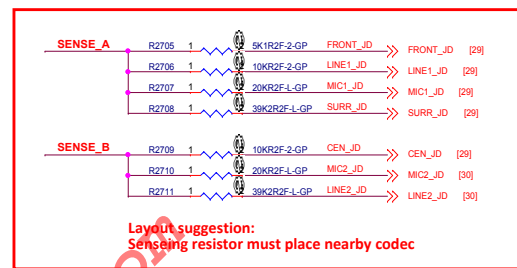


X02 Modify 0118



SYS FAN CONTROL





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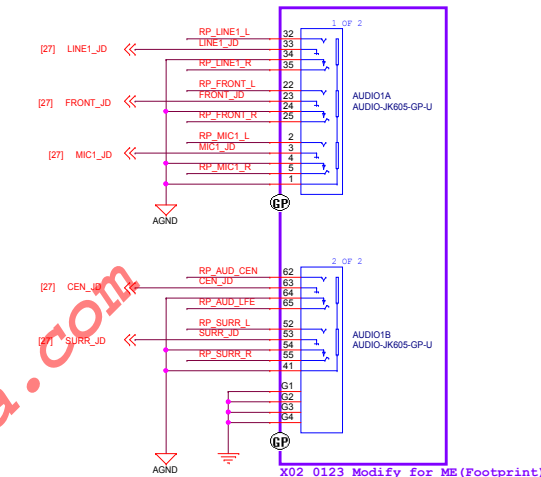
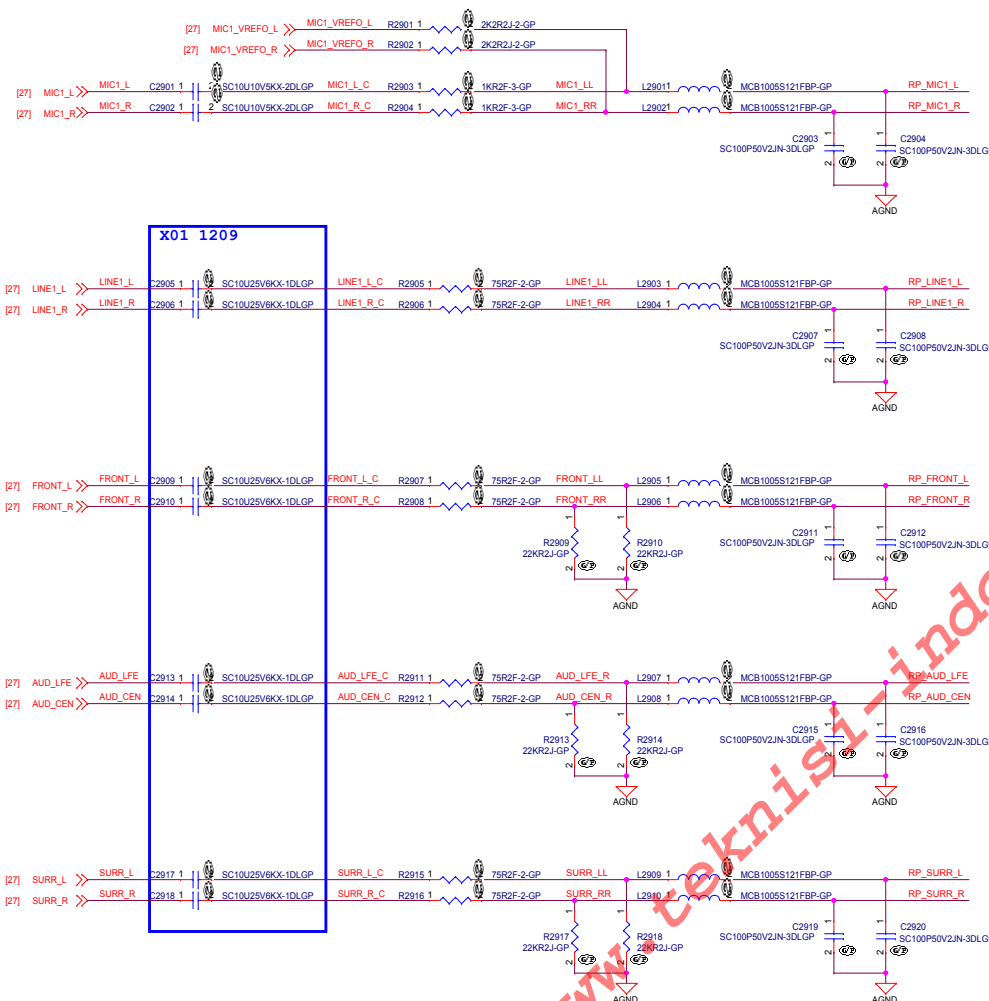
Red Skull

Rev

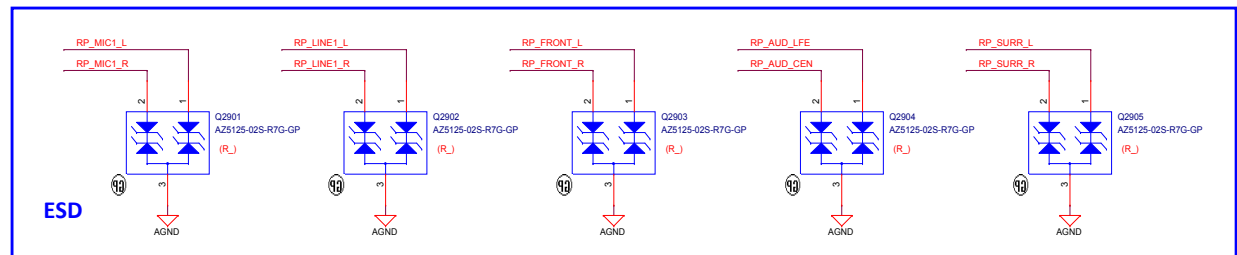
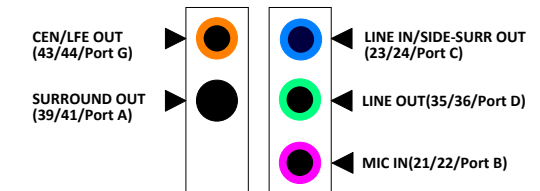
A00

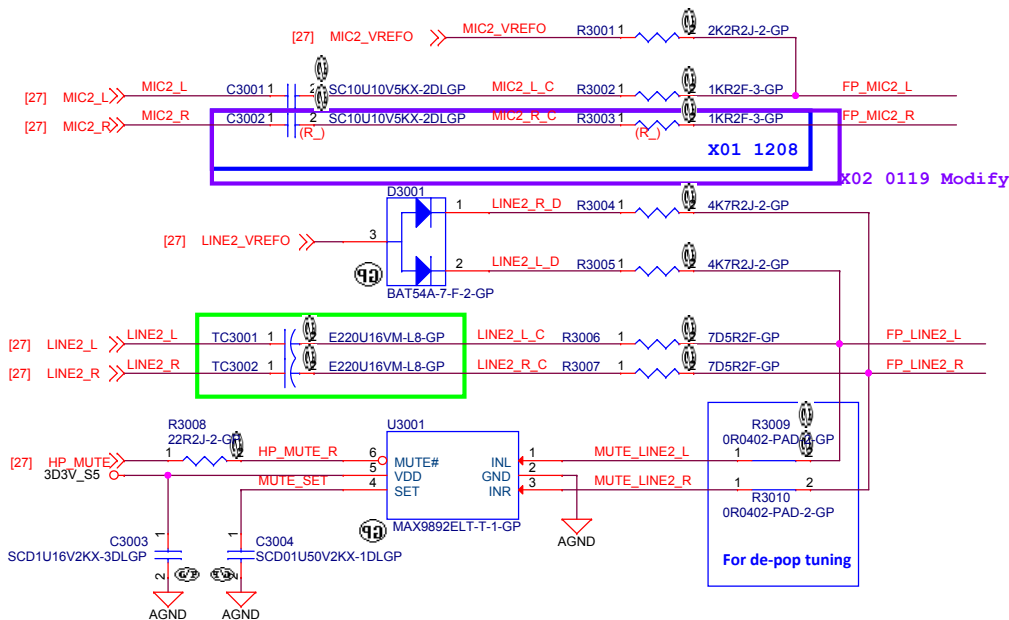
Date: Friday, March 10, 2017

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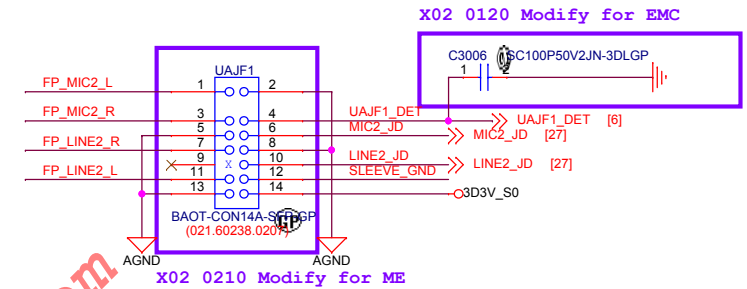


REAR PANEL PHONJACK





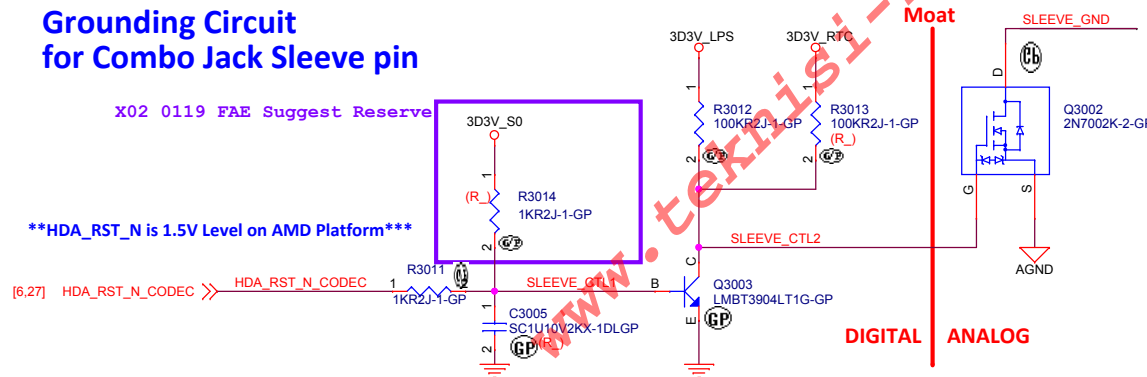
Universal Audio Jack Front Header



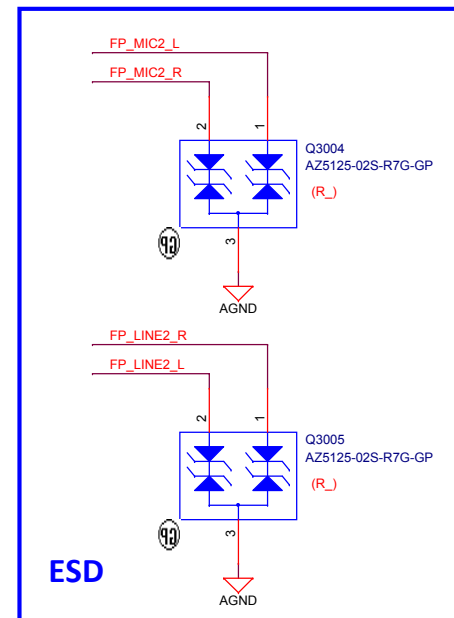
Grounding Circuit for Combo Jack Sleeve pin

X02 0119 FAE Suggest Reserve

****HDA_RST_N is 1.5V Level on AMD Platform****

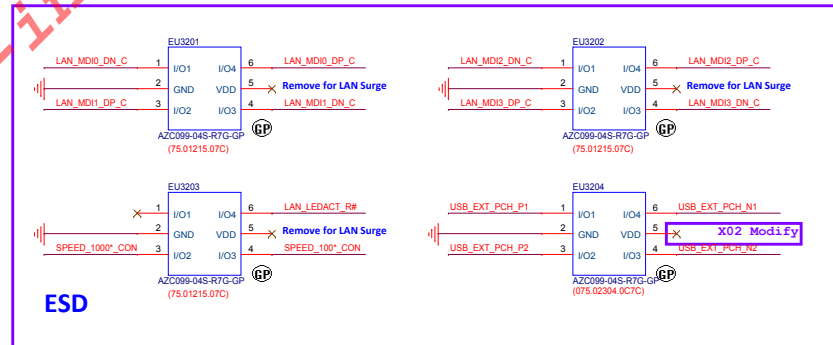
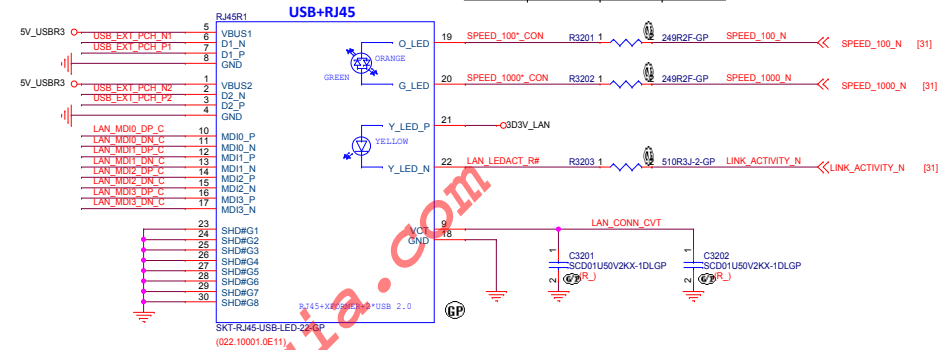


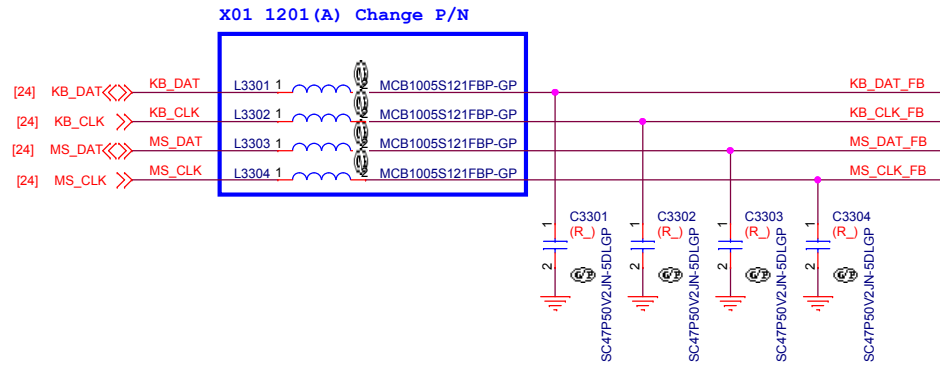
To solve the background noise while combo jack connecting to an active speaker and system entry into S3/S4/S5 without analog power.



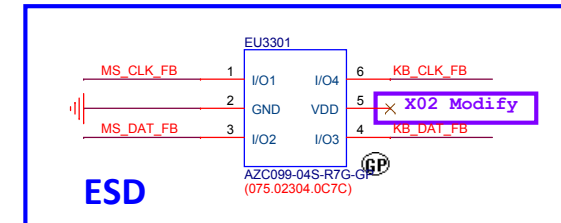
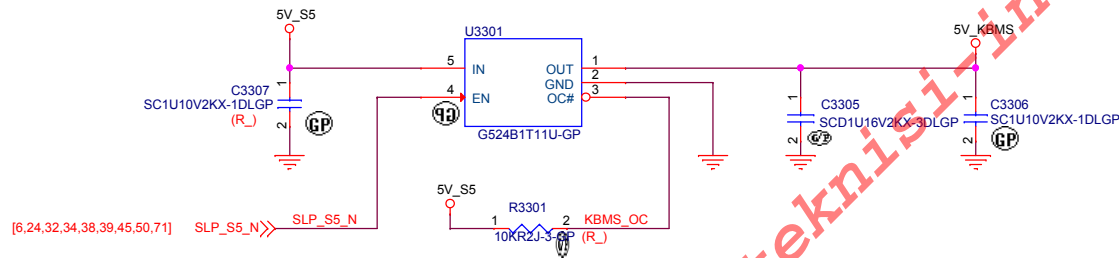
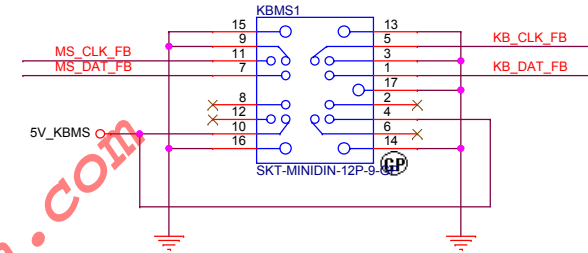
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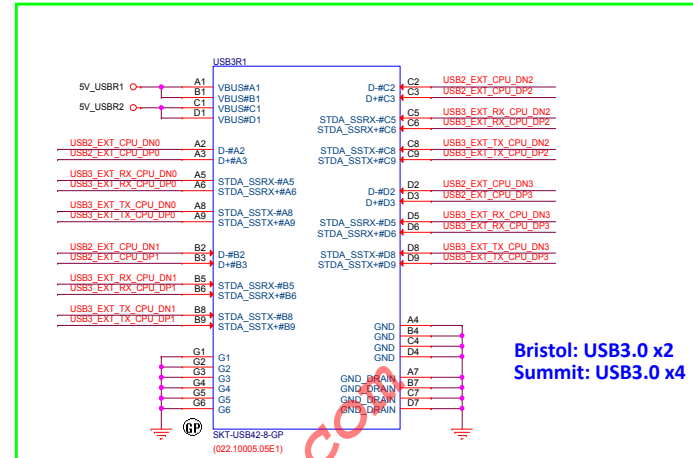
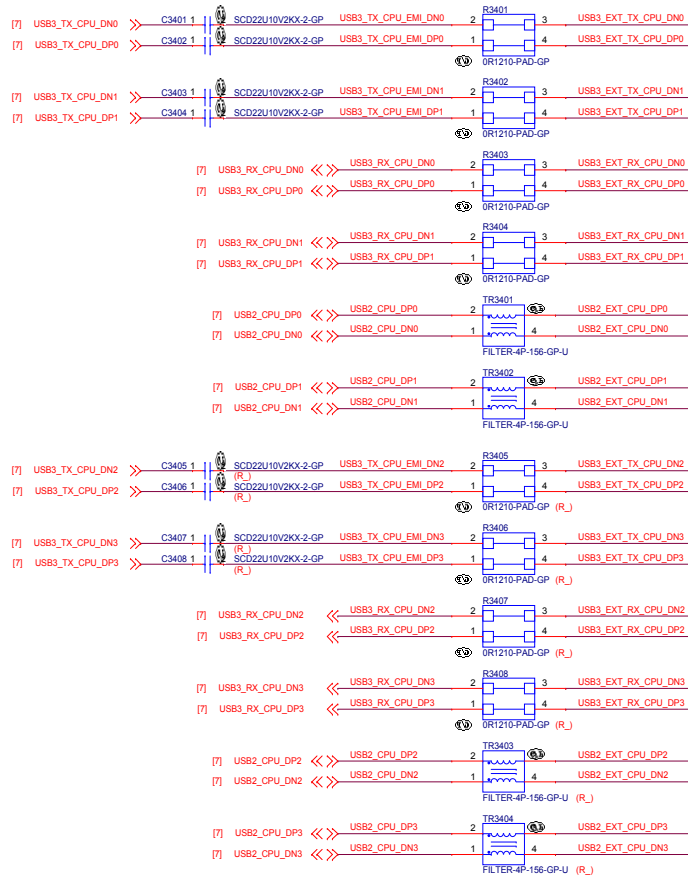
Title Audio_Front IO		
Size B	Document Number Red Skull	Rev A00
Date: Friday, March 10, 2017	Sheet 30	of 107



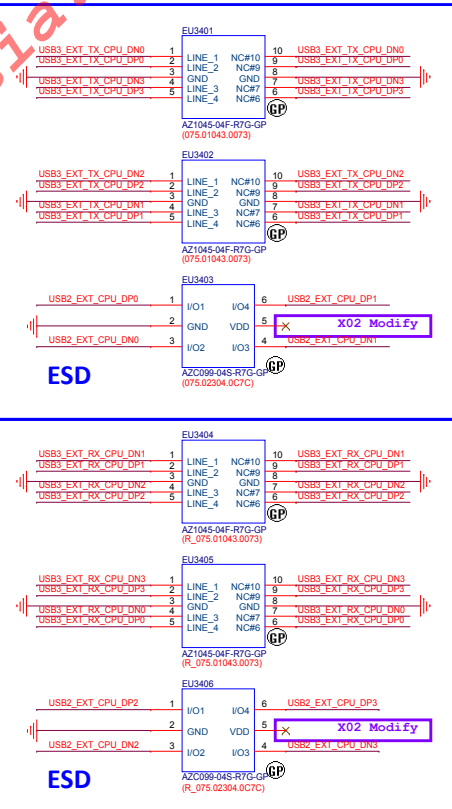


PS2 KB/MS INTERFACE





Bristol: USB3.0 x2
Summit: USB3.0 x4



ESD

ESD

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File: Rear USB3.0 Port
Size: C Document Number: Red Skull
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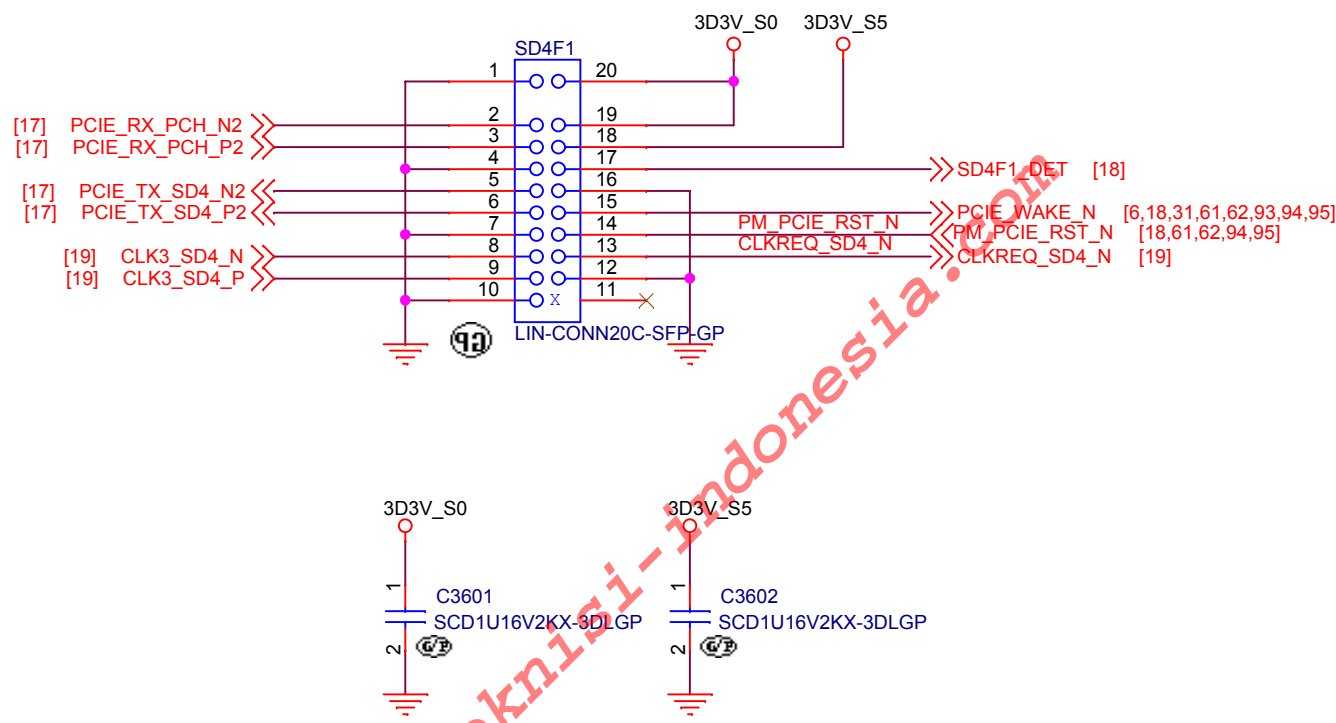
Red Skull


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Title

SD4.0 Card Reader

Size

A

Document Number

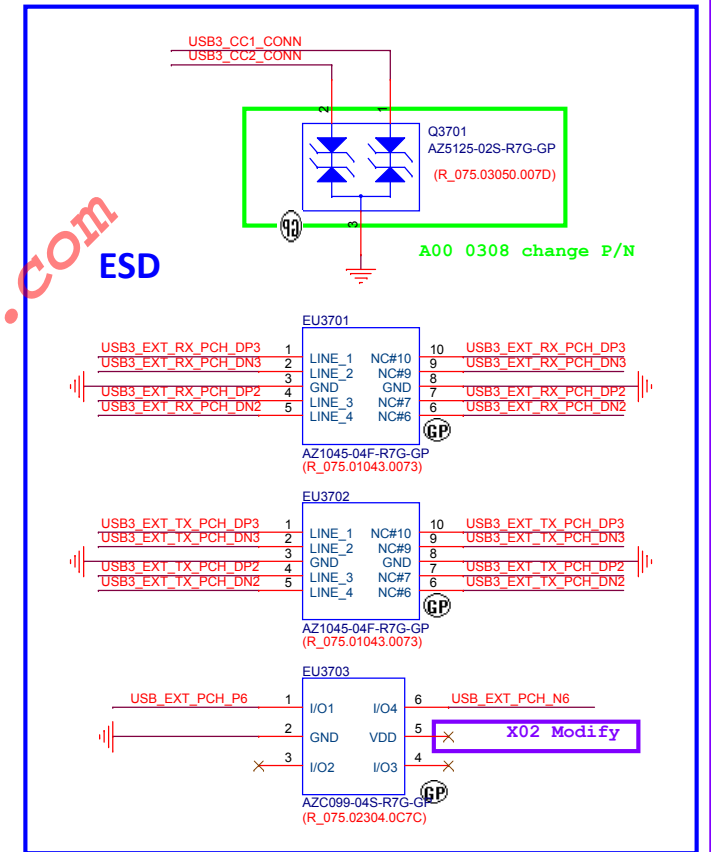
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	Title
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Front Type-C Header

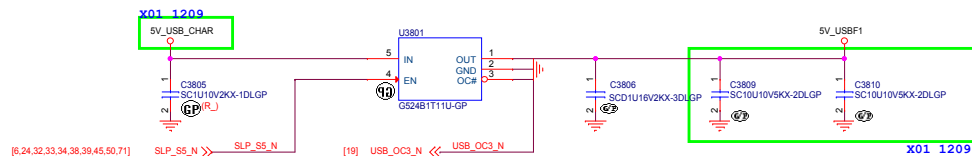
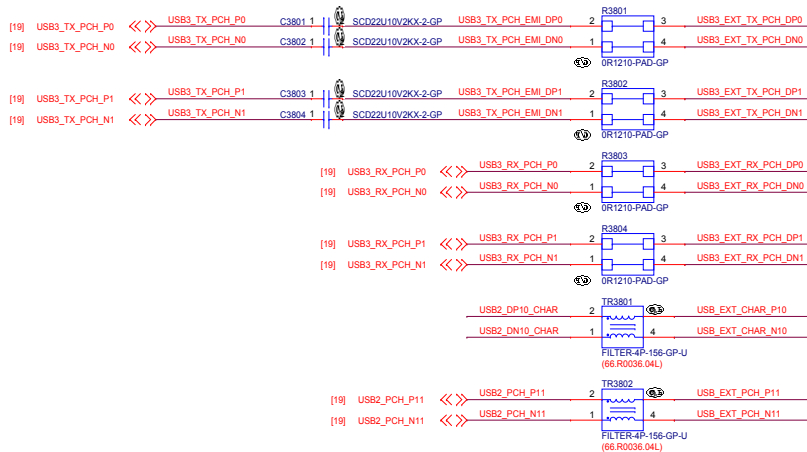
Size
B

Document Number
Red Skull

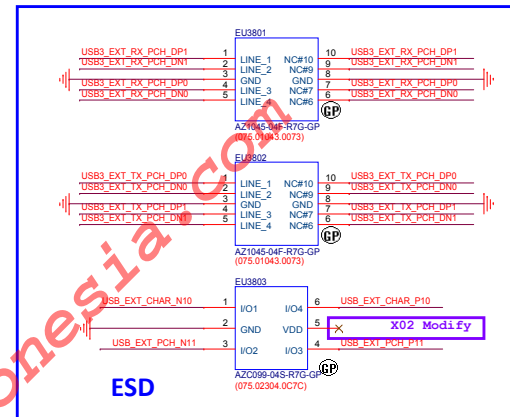
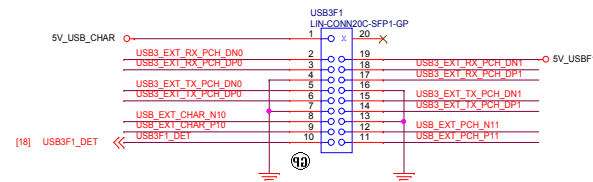
Rev
A00

Date: Friday, March 10, 2017

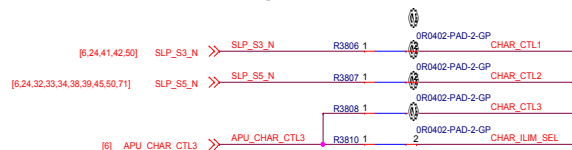
Sheet 37 of 107



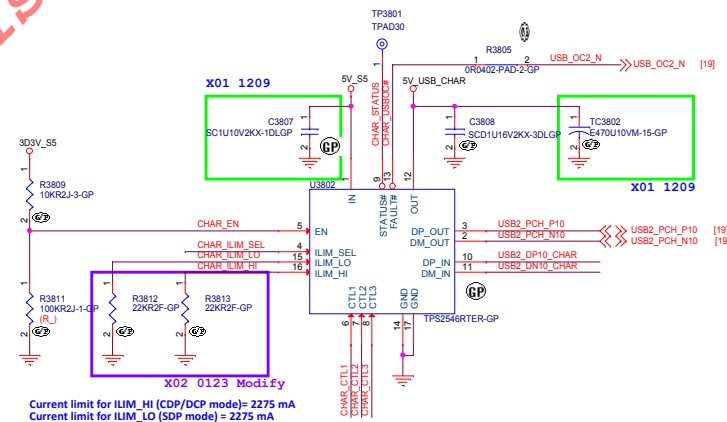
Front USB3.0 Header



Charger IC - TI TPS2546

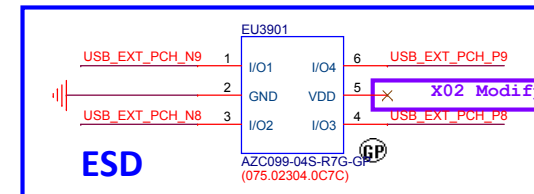
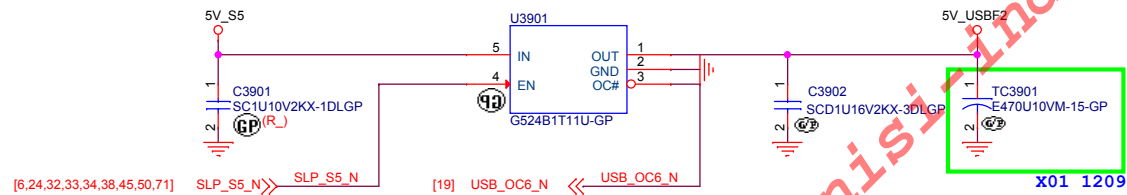
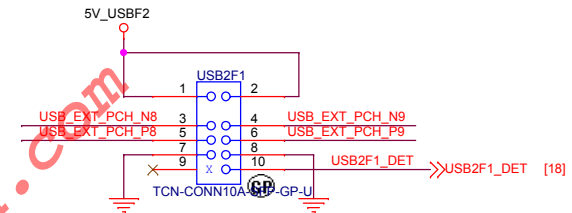
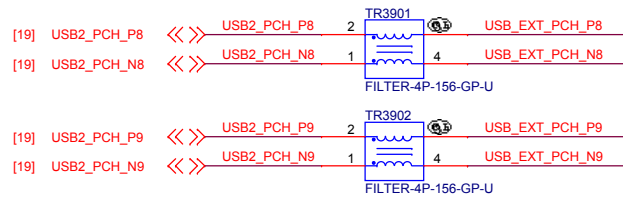


CTL1 SLP_S3#	CTL2 SLP_S4#	CTL3	ILIM_SEL	Mode	State
0	0	0	0	Turn off power switch & discharge VBUS	S4/S5
0	0	1	1	DCP	S4/S5
0	1	0	0	SDP	S3
0	1	1	1	DCP with HID auto detect USB data pass through	S3
1	1	0	0	SDP	S0
1	1	1	1	DCP	S0

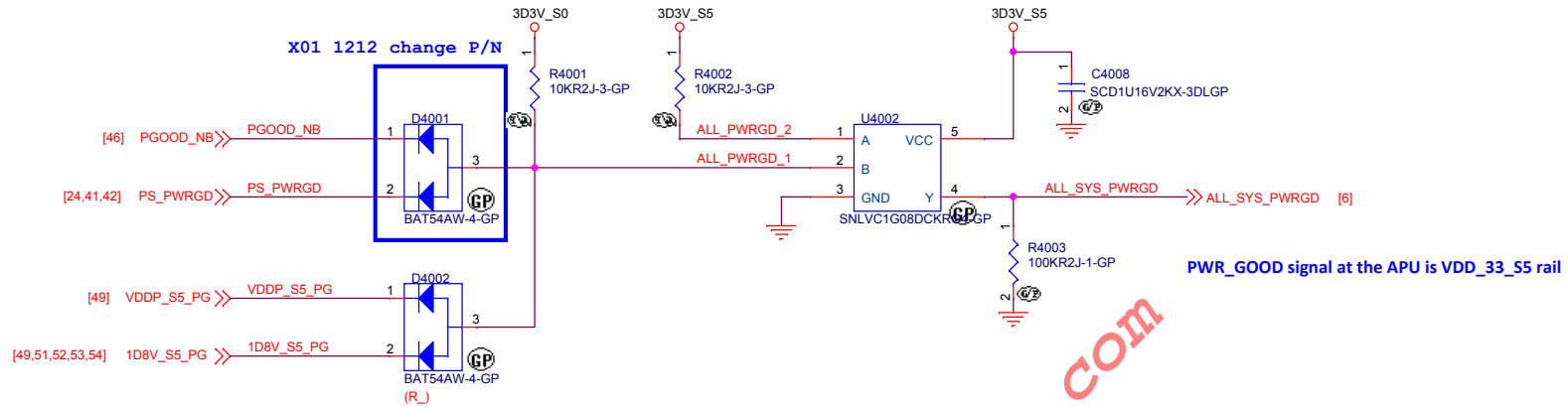


To PROMONTORY

To Connector

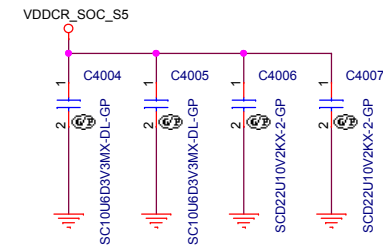
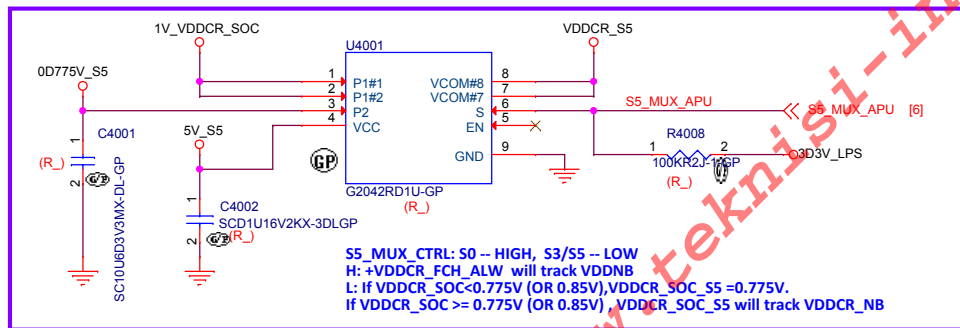


ALL_SYS_PWRGD

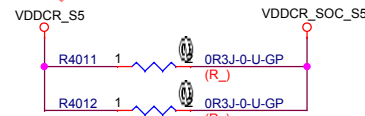


VDDCR_SOC_S5

X02 0120 Modify Unmount

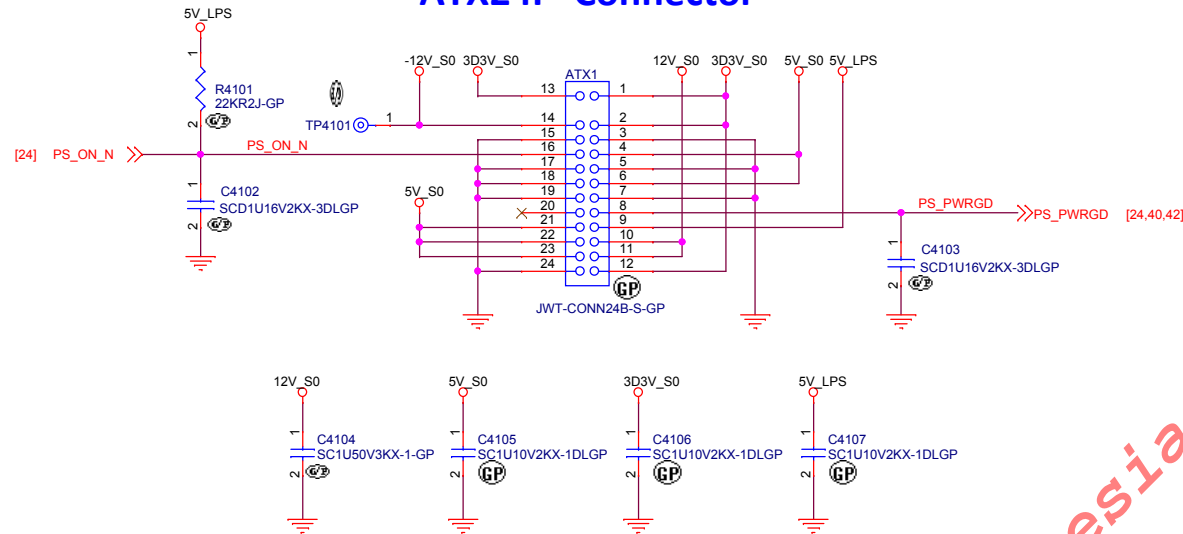


X01 1201(A)

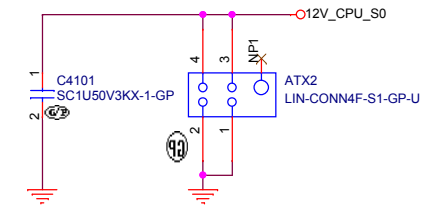


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Title Power Sequence Circuit			
Size B	Document Number Red Skull		Rev A00
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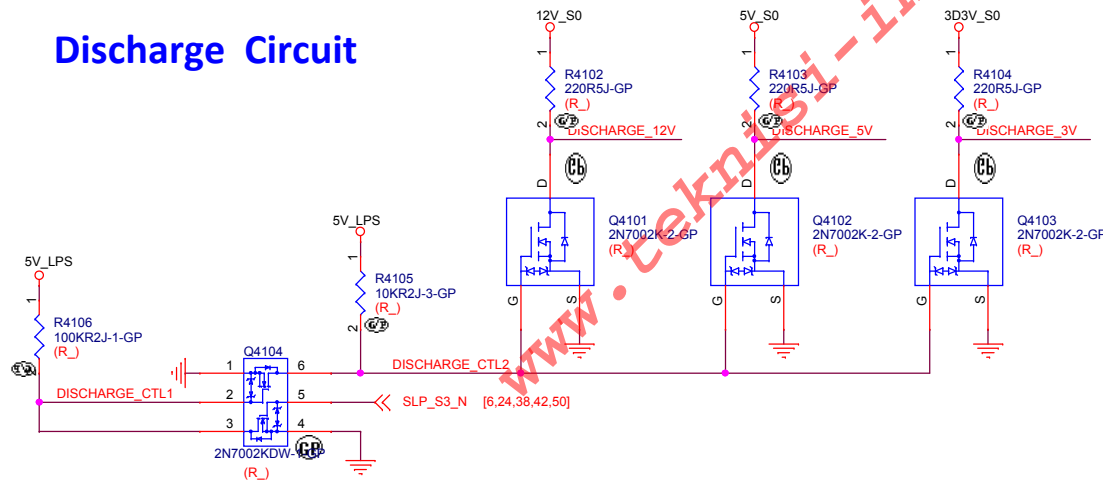
ATX24P Connector

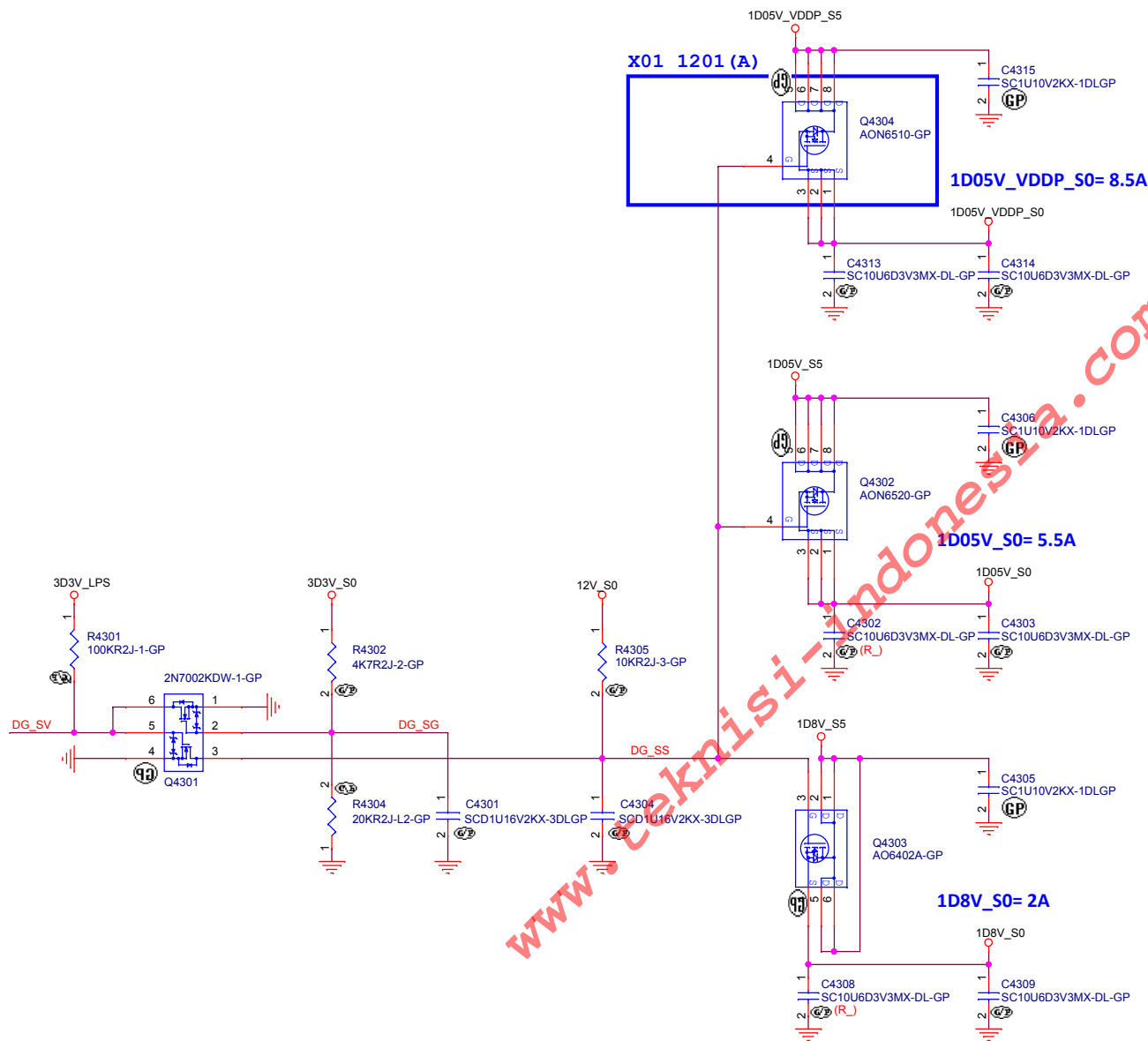


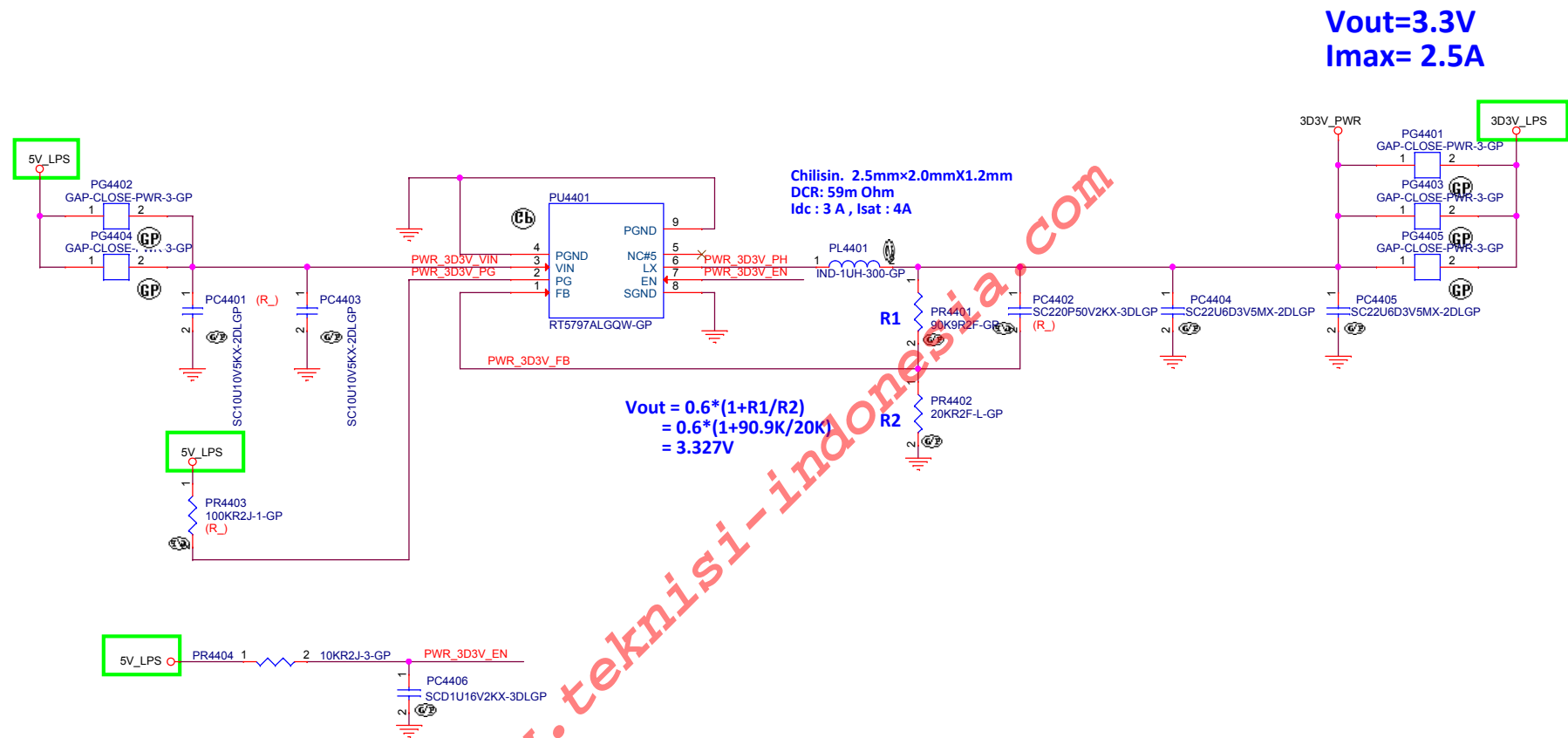
ATX4P CPU Connector



Discharge Circuit

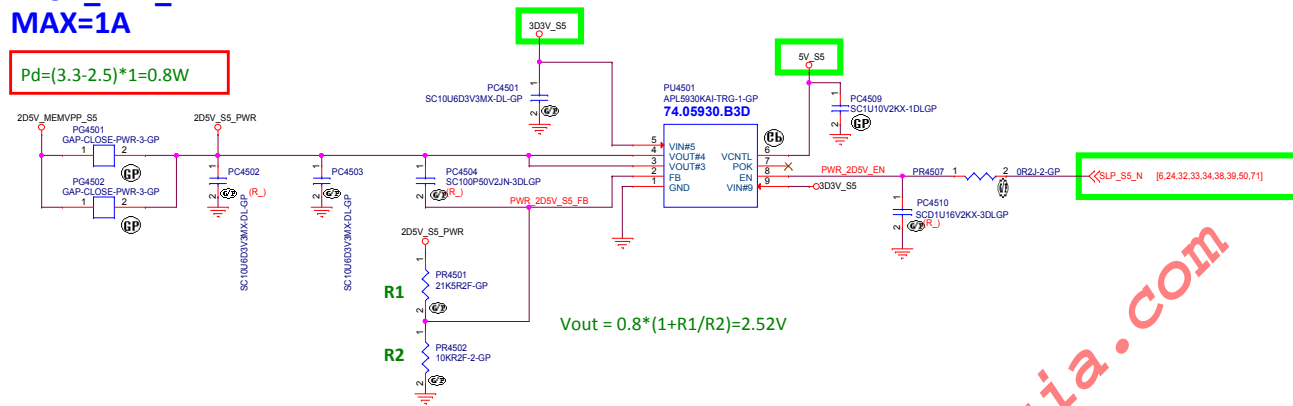






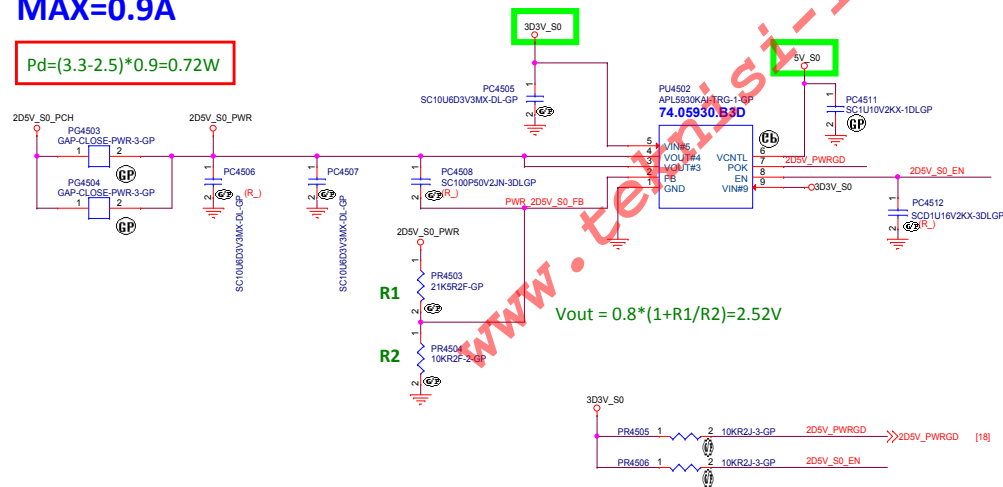
2D5V_VPP_MEM MAX=1A

$$Pd = (3.3 - 2.5) * 1 = 0.8W$$



PROM 2D5V_S0 MAX=0.9A

$$Pd = (3.3 - 2.5) * 0.9 = 0.72W$$



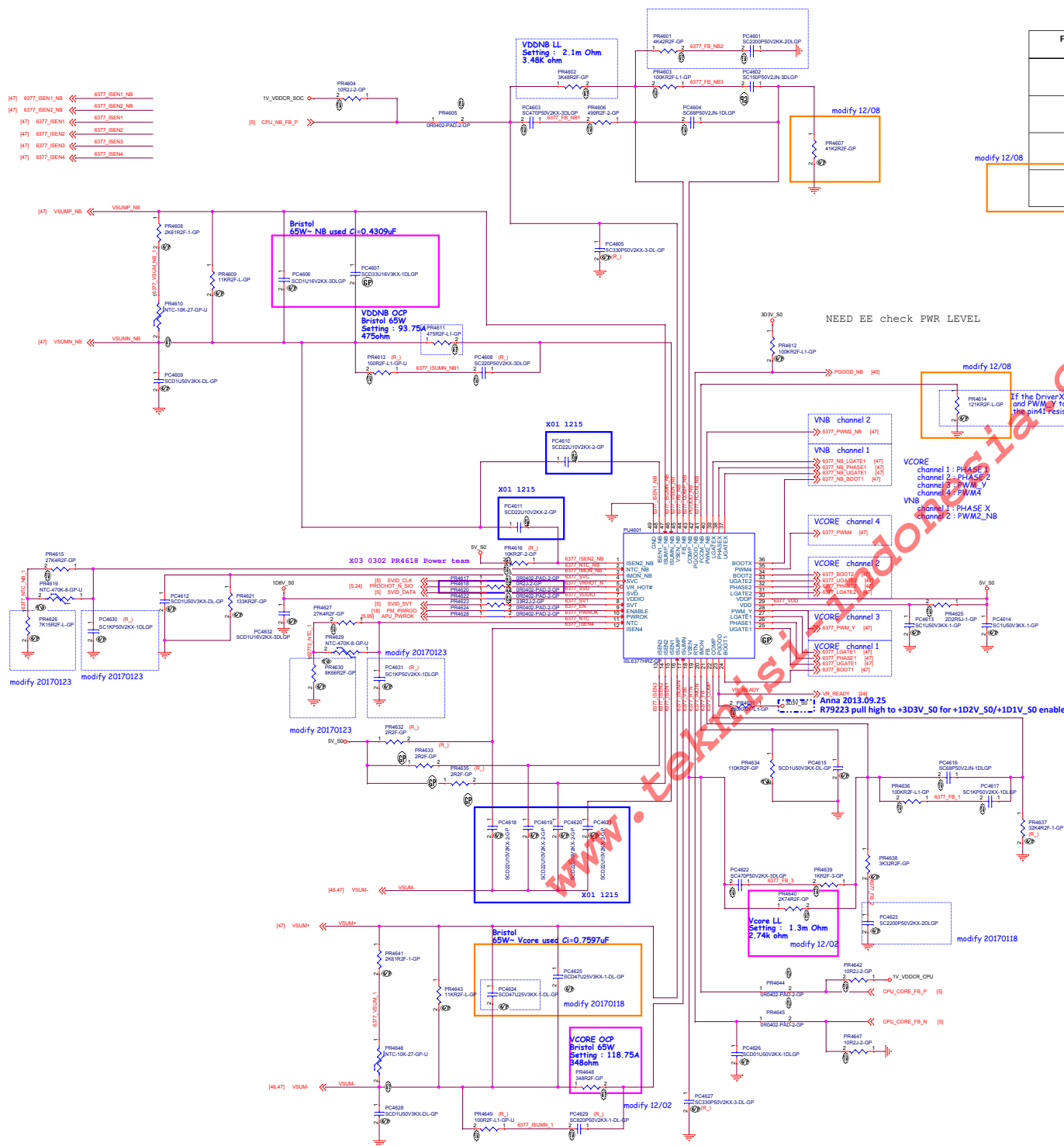


TABLE 5. SWITCHING FREQUENCY SELECTION

FREQUENCY [kHz]	COMP_NB RANGE [kΩ]	FCCM_NB RANGE [kΩ]
300	57.6 to OPEN	19.1 to 41.2 or 154 to OPEN
350	5.62 to 41.2	19.1 to 41.2 or 154 to OPEN
400	57.6 to OPEN	5.62 to 16.9 or 57.6 to 121
450	5.62 to 41.2	5.62 to 16.9 or 57.6 to 121

Setting by PR4607 Setting by PR4614

TABLE 4. FCCM_NB RESISTOR SELECTION

RESISTOR VALUE [kΩ]	SLEW RATE FOR CORE AND NORTHBRIDGE [mV/μs]	DriverX	PWM_Y
5.62	20	Core VR Channel 3	NB VR Channel 1
7.87	15		
11.5	12.5		
16.9	10		
19.6	20		
24.9	15		
34.0	12.5		
41.2	10		
52.3	20		
73.2	15		
95.3	12.5		
121	10	NB VR Channel 1	Core VR Channel 3
154	20	NB VR Channel 1	Core VR Channel 3
182	15		
210	12.5		
OPEN	10		

Setting by PR4614

Summit:
VDD CORE 1.5V/80A(TDC) 125A(EDC) (95W)
VDD CORE 1.5V/60A(TDC) 90A(EDC) (65W)
Summit:
VDDNB 1.2V/20A(TDC) 30A(EDC) (95W and 65W)

Bristol:
VDD CORE 1.5V/65A(TDC) 95A(EDC) (65W)
Bristol:
VDDNB 1.2V/50A(TDC) 75A(EDC) (65W)

OVP: If the VSEN voltage exceeds
Vp & 50mV
the output voltage VID value plus
any programmed offsets by +35mV,
the controller declares an overvoltage fault

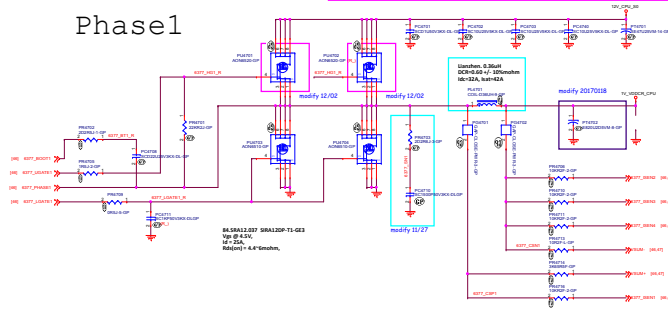
Summit:
VDD CORE 1.5V/80A(TDC) 125A(EDC) (95W)
VDD CORE 1.5V/60A(TDC) 90A(EDC) (65W)

Bristol:
VDD CORE 1.5V/65A(TDC) 95A(EDC) (65W)

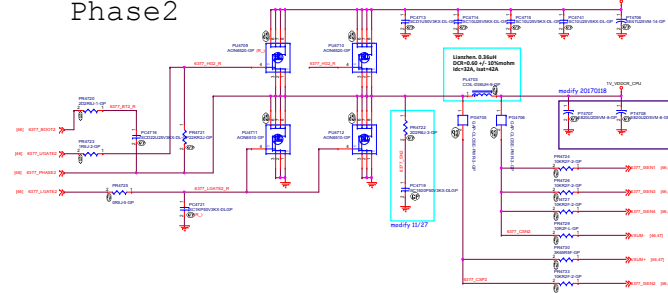
Summit:
VDDNB 1.2V/20A(TDC) 30A(EDC) (95W and 65W)

Bristol:
VDDNB 1.2V/50A(TDC) 75A(EDC) (65W)

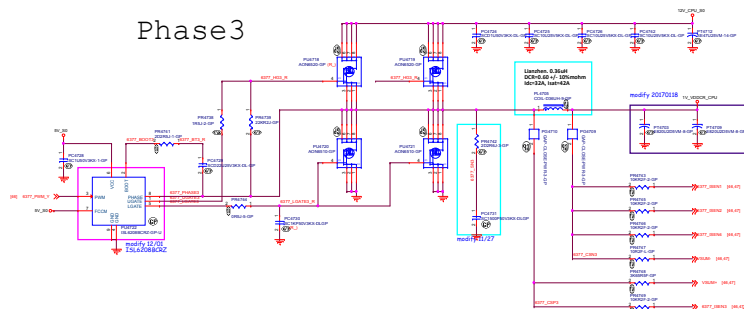
Phase1



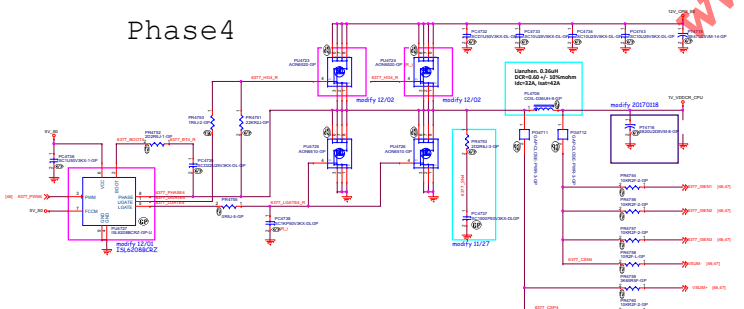
Phase2



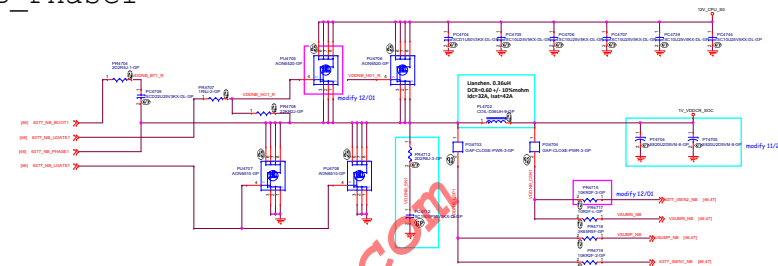
Phase3



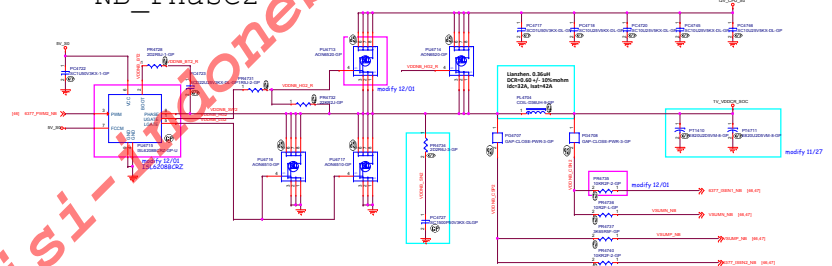
Phase4



NB_Phase1



NB_Phase2



Summit
95W
TDC = 80 A
EDC = 125 A
EDC*1.25 = OCP > 156.25 A
65W
TDC = 60 A
EDC = 90 A
OCP > 112.5 A

Bristol
65W
TDC = 65 A
EDP = 95 A
OCP > 118.75 A

Summit
95W and 65W
TDC = 20 A
EDP = 30 A
OCP > 37.5 A

Bristol
65W
TDC = 50 A
EDP = 75 A
OCP > 93.75 A

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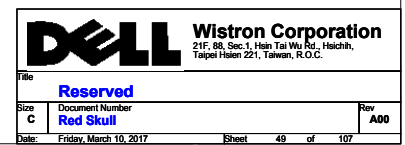
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Bristol Ridge: 1.05V/9.5A
Summit Ridge: 0.9V/1A



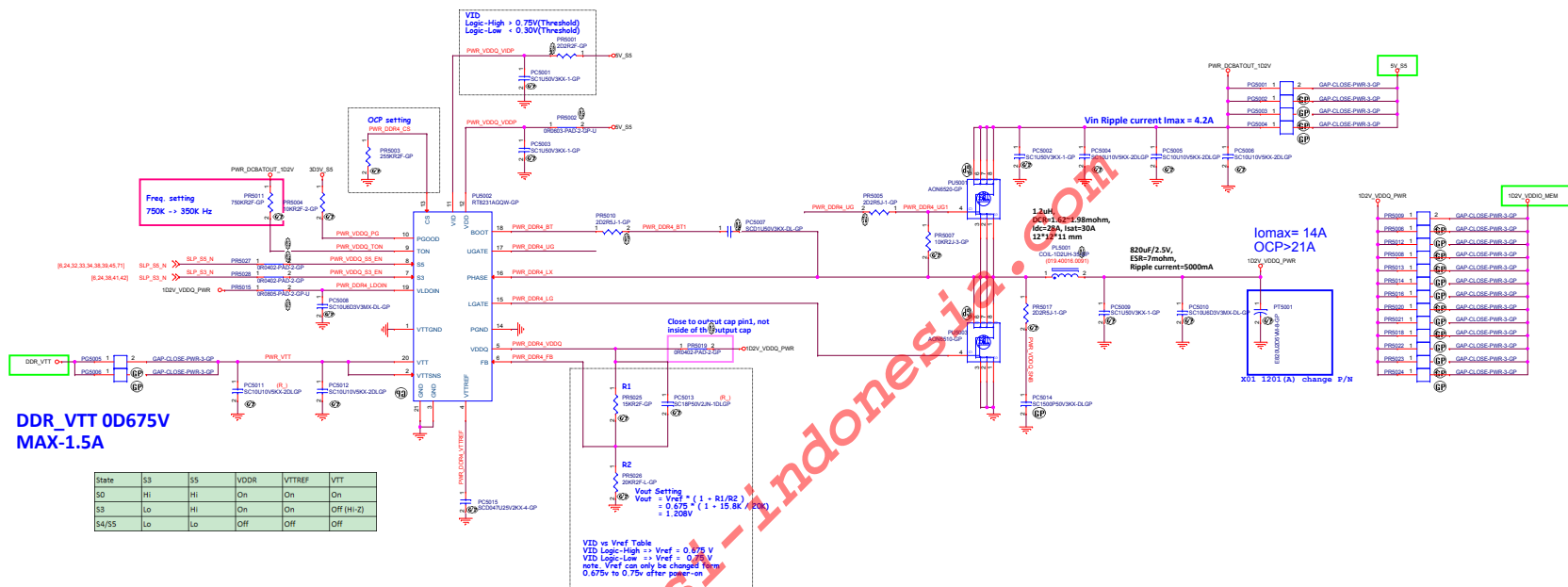


Table 2. S3 and S5 truth table

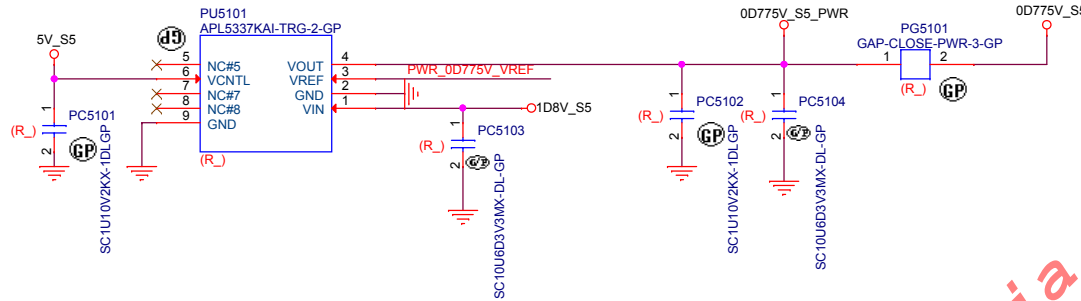
STATE	S3	S5	VDDQ	VTTREF	VTT
S0	Hi	Hi	On	On	On
S3	Lo	Hi	On	On	Off (Hi-Z)
S4/S5	Lo	Lo	Off	Off	Off

Table 1. VID and Reference Voltage Setting

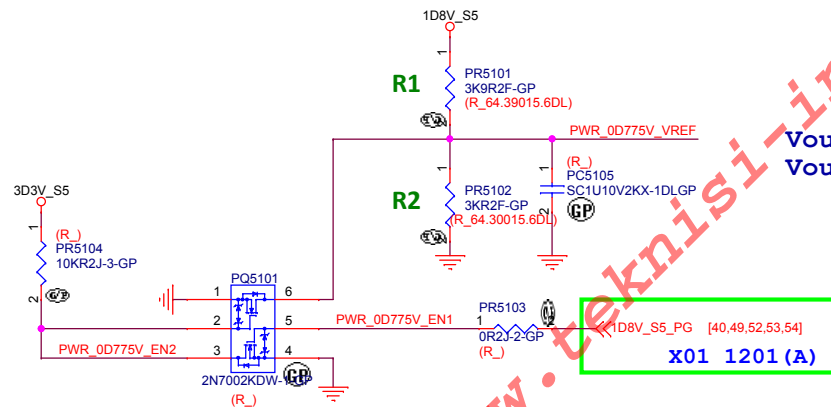
VID	Reference Voltage (V)
High	0.675
Low	0.75

0D775V_S5 MAX=0.2A

$$Pd=(1.8-0.775)*0.2=0.205W$$



Bristol Ridge only



Vout Setting

$$Vout = 1.8 * R1 / (R1+R2)$$

$$Vout = 1.8 * (3k / (3.9k+3k))$$

$$Vout = 0.782 V$$

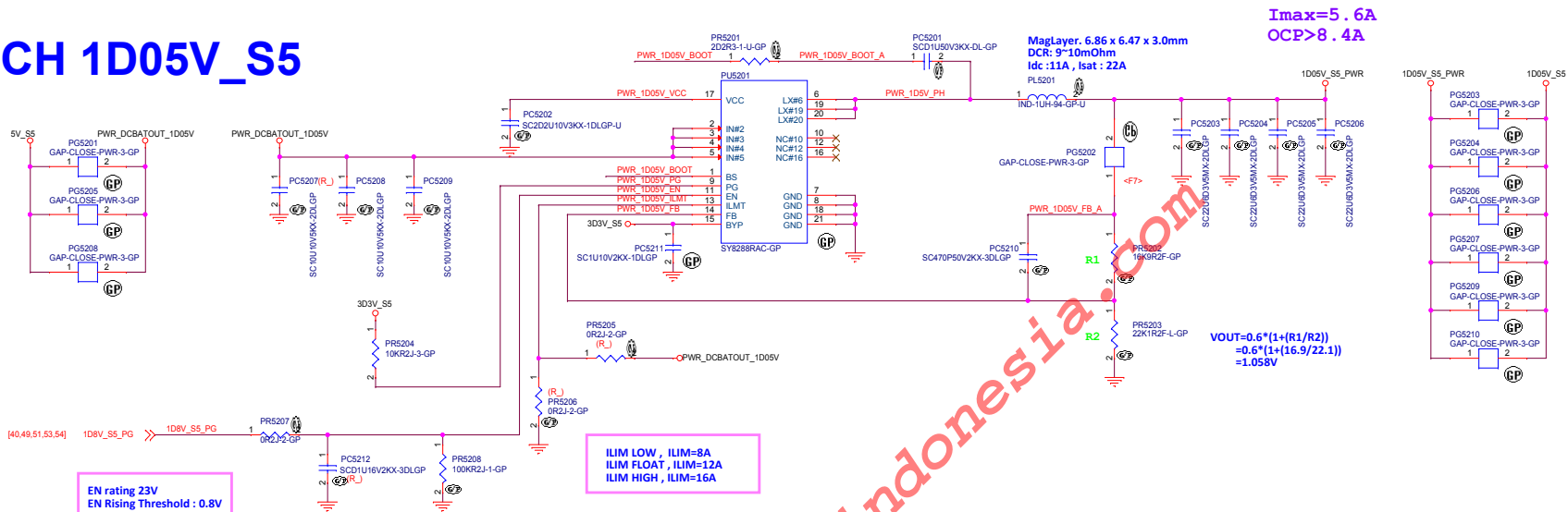
X01 1201 (A)

X02 0207 Unmount

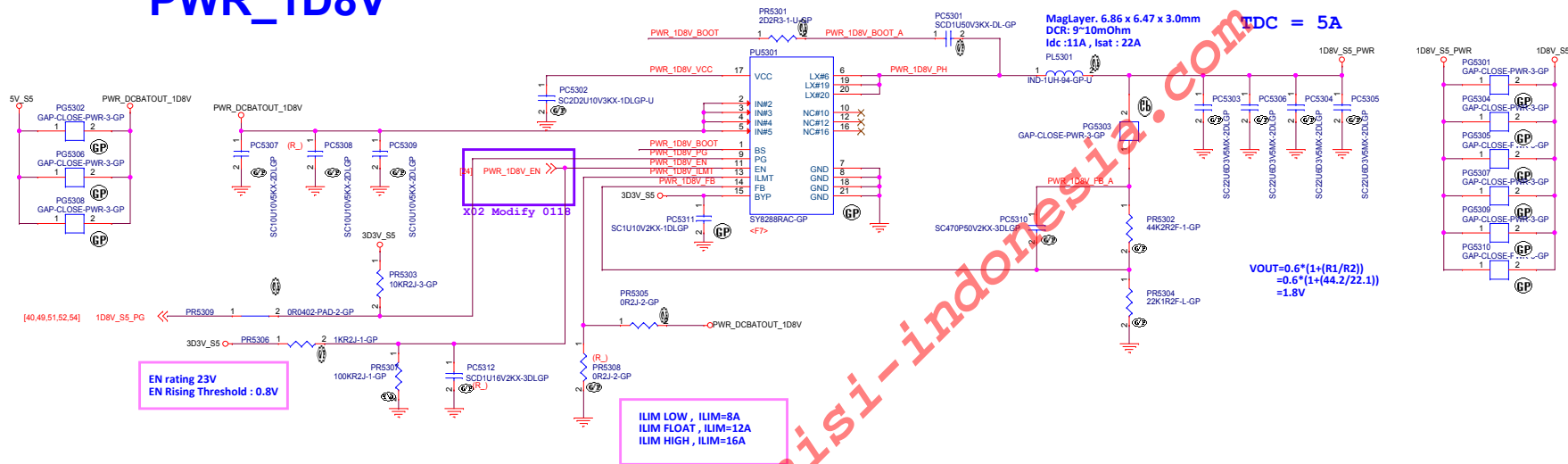
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FCH 1D05V_S5



PWR_1D8V



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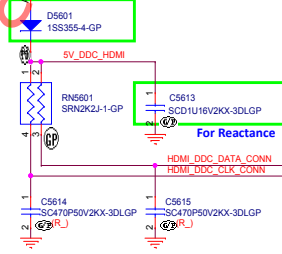
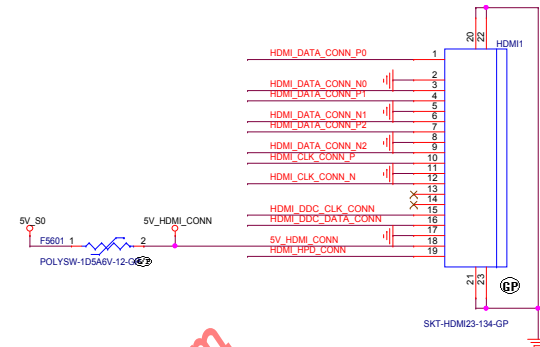
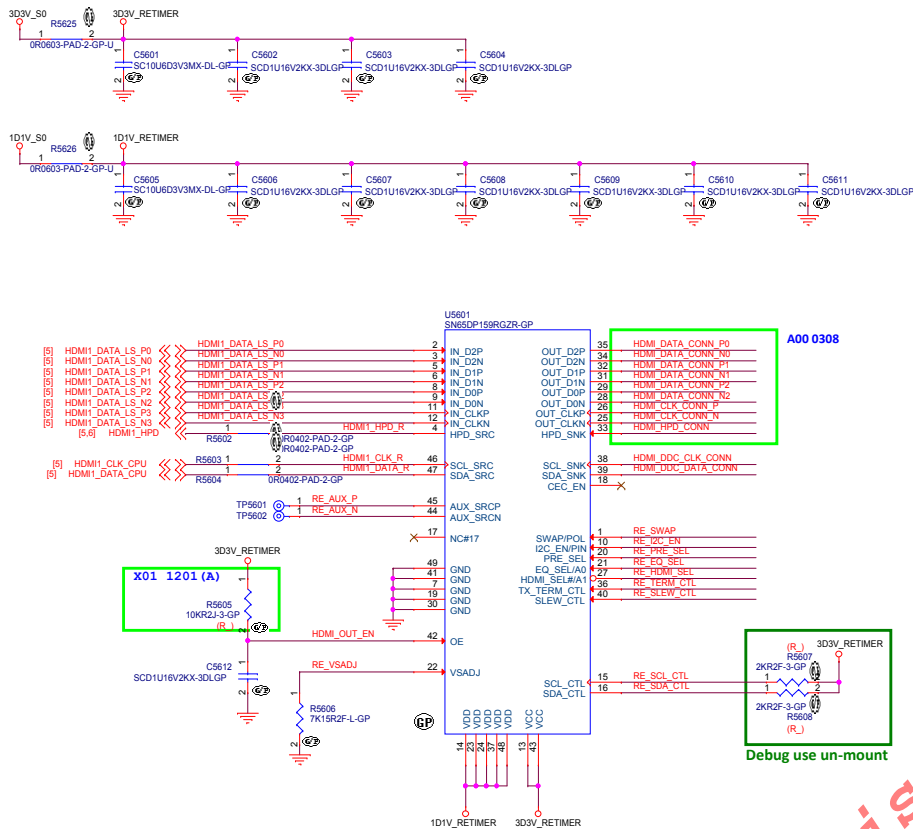
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**A00 0308 Modify
Delete CMC and ESD for Impedance Issue**

SWAPPOL	1	NA	3 level (1)
Input lane SWAP and polarity control pin when I2C_EN/PIN = Low SWAPPOL = H: receive lane polarity swap (retimer mode only) SWAPPOL = L: receive lanes swap (retimer and retidriver mode) SWAPPOL = No Connect: normal working			
HDMI_SELA1	27	23	1
HDMI_SEL = High: Device configured for DVI HDMI_SEL = Low: Device configured for HDMI (Adaptor ID block is readable through I2C or I2C-over-AUX) When I2C_EN/PIN = High Address 0x2 Note: Weak internal pull down Transmit Termination Control when I2C_EN/PIN = Low TX_TERM_CTL = L: No transmit termination TX_TERM_CTL = H: Transmit termination impedance in 75 to about 150 Ω TX_TERM_CTL = No Connect: automatically selects the termination impedance Data rate (DR) > 3.4 Gbps ~ 75 to 100 Ω differential near end termination 2 Gbps ~ DR < 3.4 Gbps ~ 150 to 300 Ω differential near end termination DR < 2 Gbps ~ no termination Note: Left floating will be in automatic select mode.			
TX_TERM_CTL	36	N/A	3 level (1)

SLEW_CTL	40	34	3 level (1)
Slew rate control when I2C_EN/PIN = Low SLEW_CTL = H: fastest data rate SLEW_CTL = L: 5 ps slow SLEW_CTL = No Connect: 10 ps slow When I2C_EN/PIN = High Slew rate is controlled through I2C			
PRE_SEL	20	16	3 level (1)
De-emphasis pin strap when I2C_EN/PIN = Low PRE_SEL = L: 2 dB de-emphasis PRE_SEL = No Connect: 0 dB PRE_SEL = H: Reserved			
EQ_SEL/AO	21	17	3 level (1)
Input Receive Equalization pin strap when I2C_EN/PIN = Low EQ_SEL = L: Fixed EQ at 7.5 dB EQ_SEL = No Connect: Adaptive EQ EQ_SEL = H: Fixed at 14 dB When I2C_EN/PIN = High Address 0x1 Note: (3 level for pin strap programming but 2 level when I2C address)			
I2C_EN/PIN	10	8	1
I2C_EN/PIN = High: puts device into I2C control mode I2C_EN/PIN = Low: puts device into pin strap mode			

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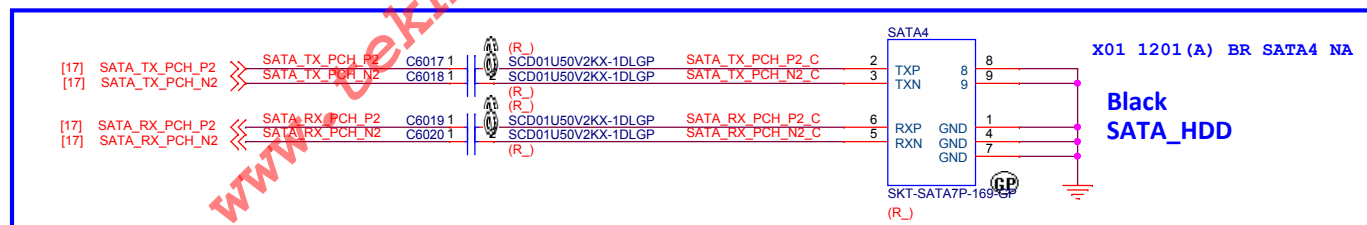
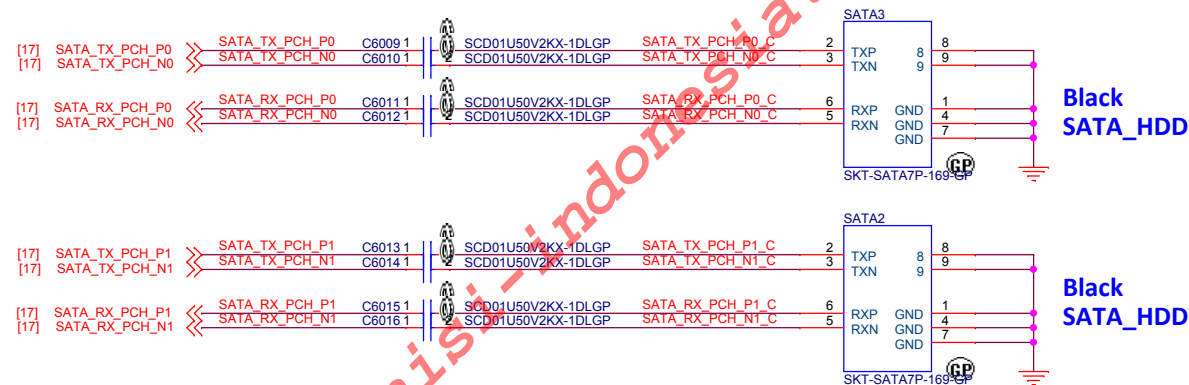
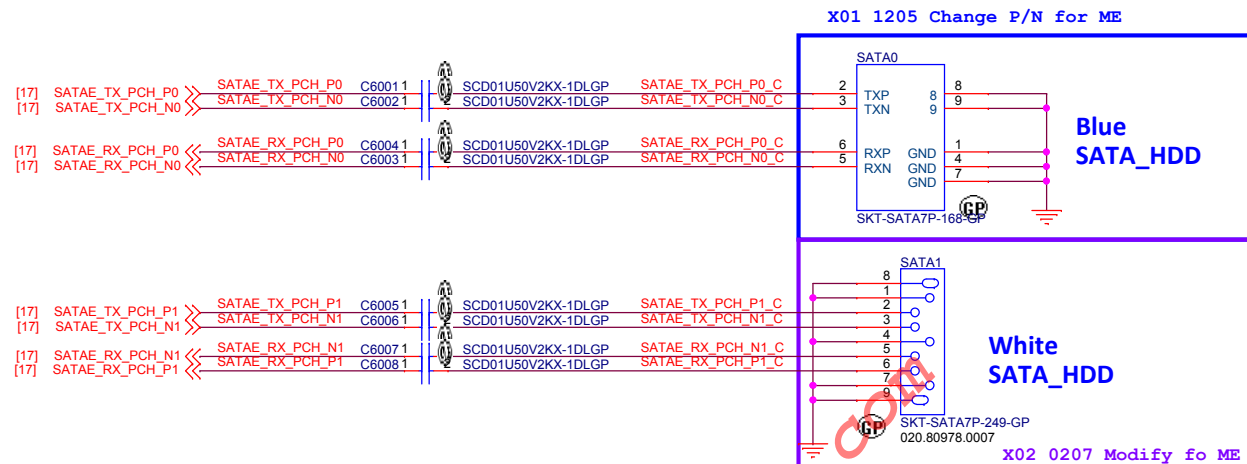
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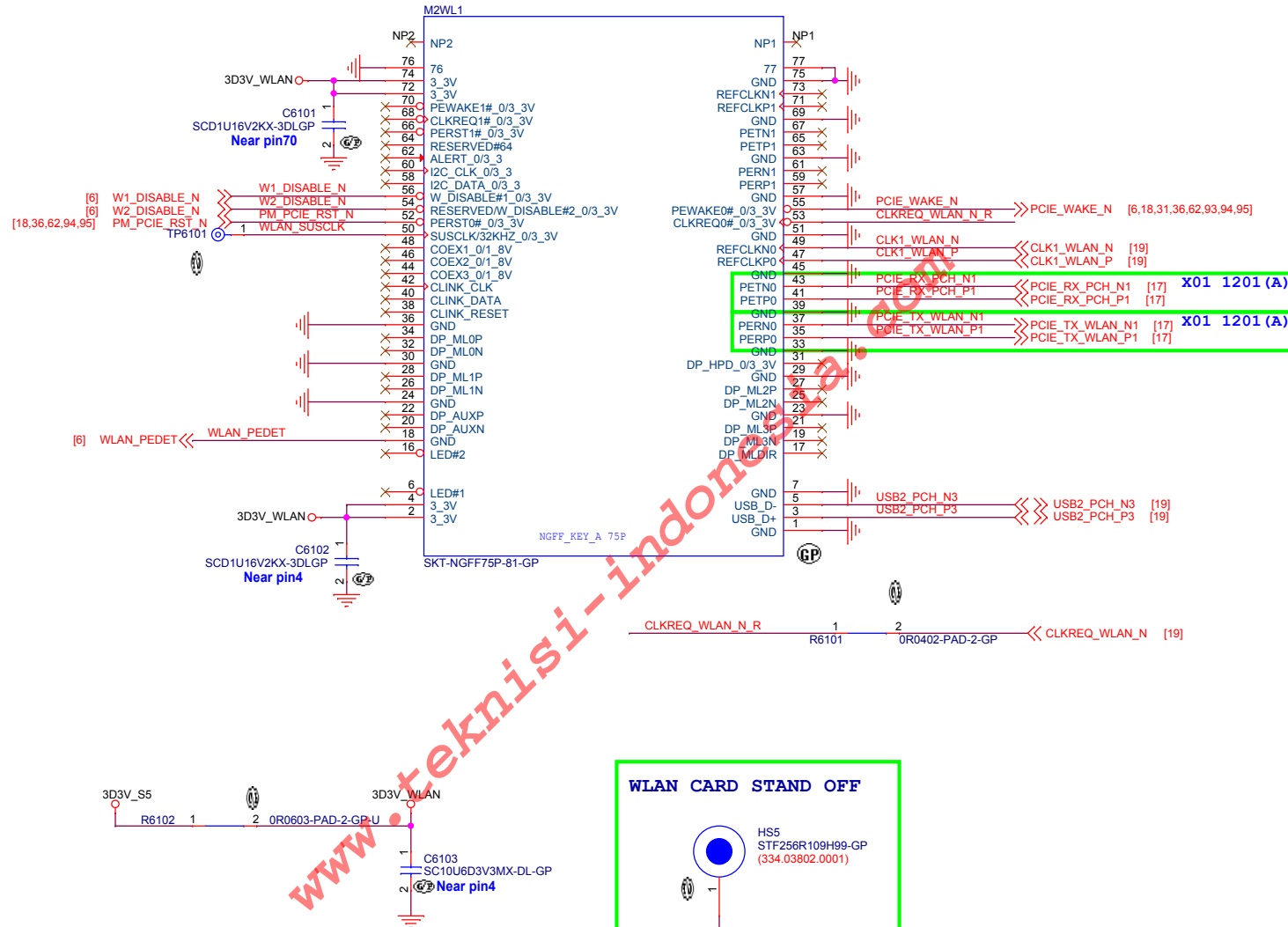
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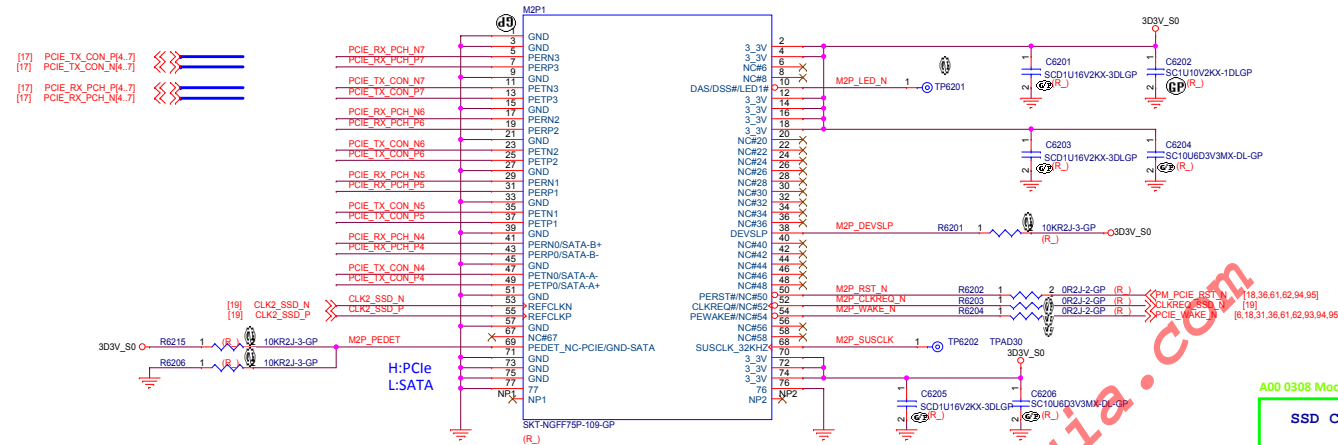


H: 4.2mm

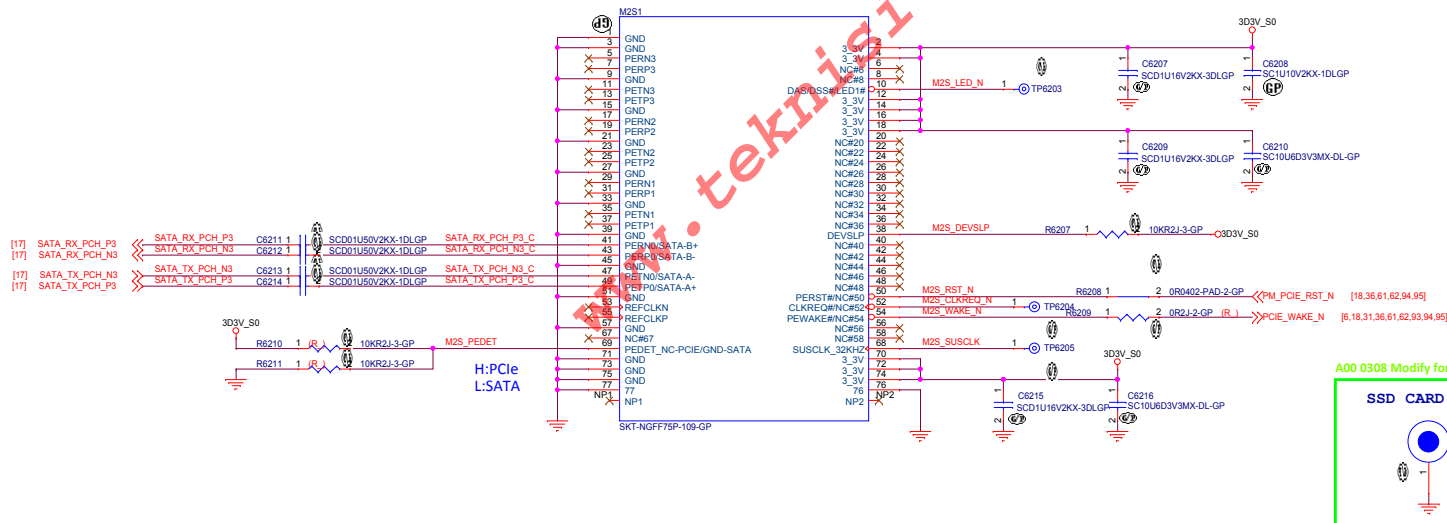


M.2 2280 Key M Type (PCIe x4 Only)

X01 1201 (A) BR M2P1 NA



M.2 2280 Key M Type (SATA Only)



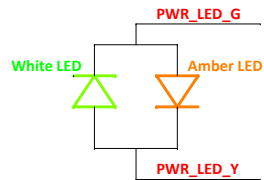
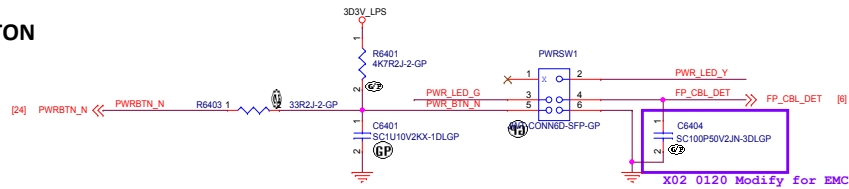
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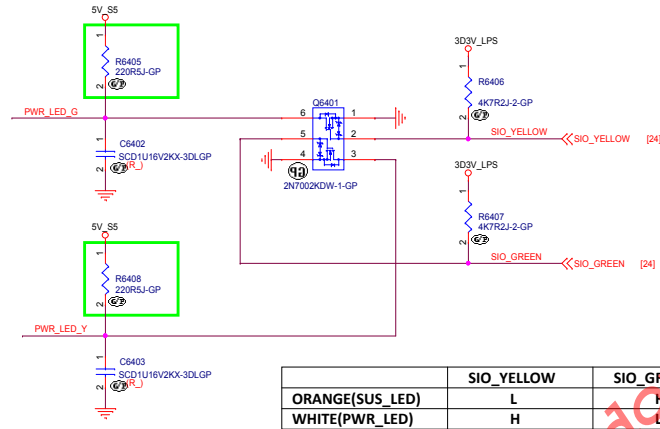
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POWER BUTTON

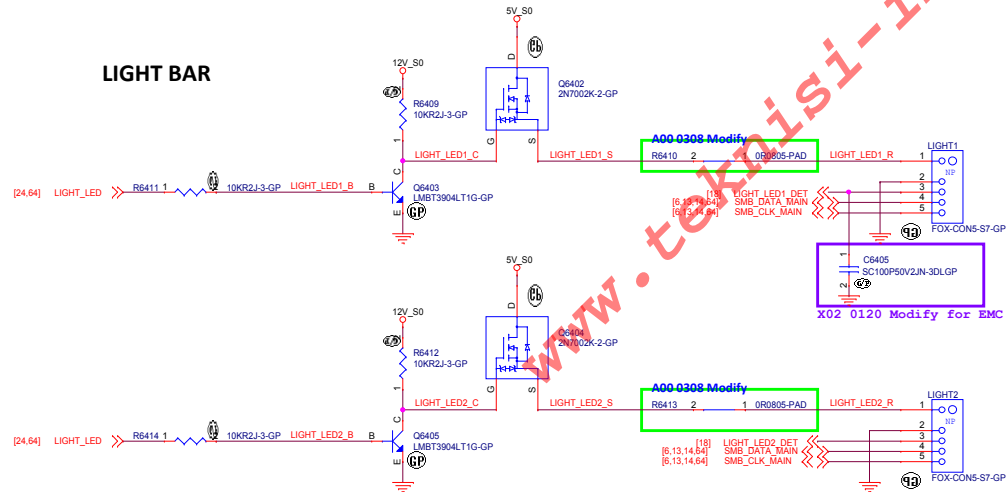


S0	White
S3	White(blinking)
S4/S5	LED off
No Post	Amber
Failure to Post	Amber(blinking)



	SIO_YELLOW	SIO_GREEN
ORANGE(SUS_LED)	L	H
WHITE(PWR_LED)	H	L

LIGHT BAR



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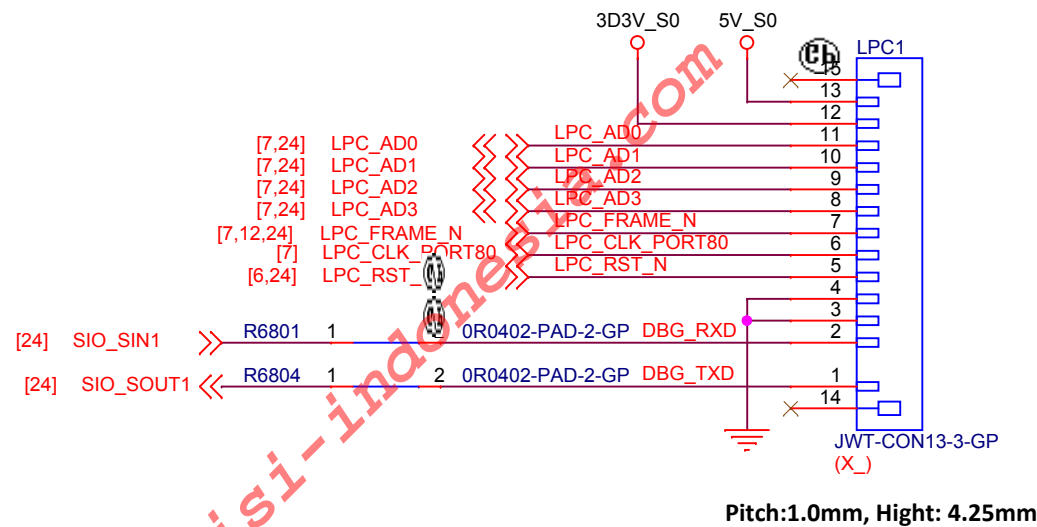
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LPC DEBUG PORT






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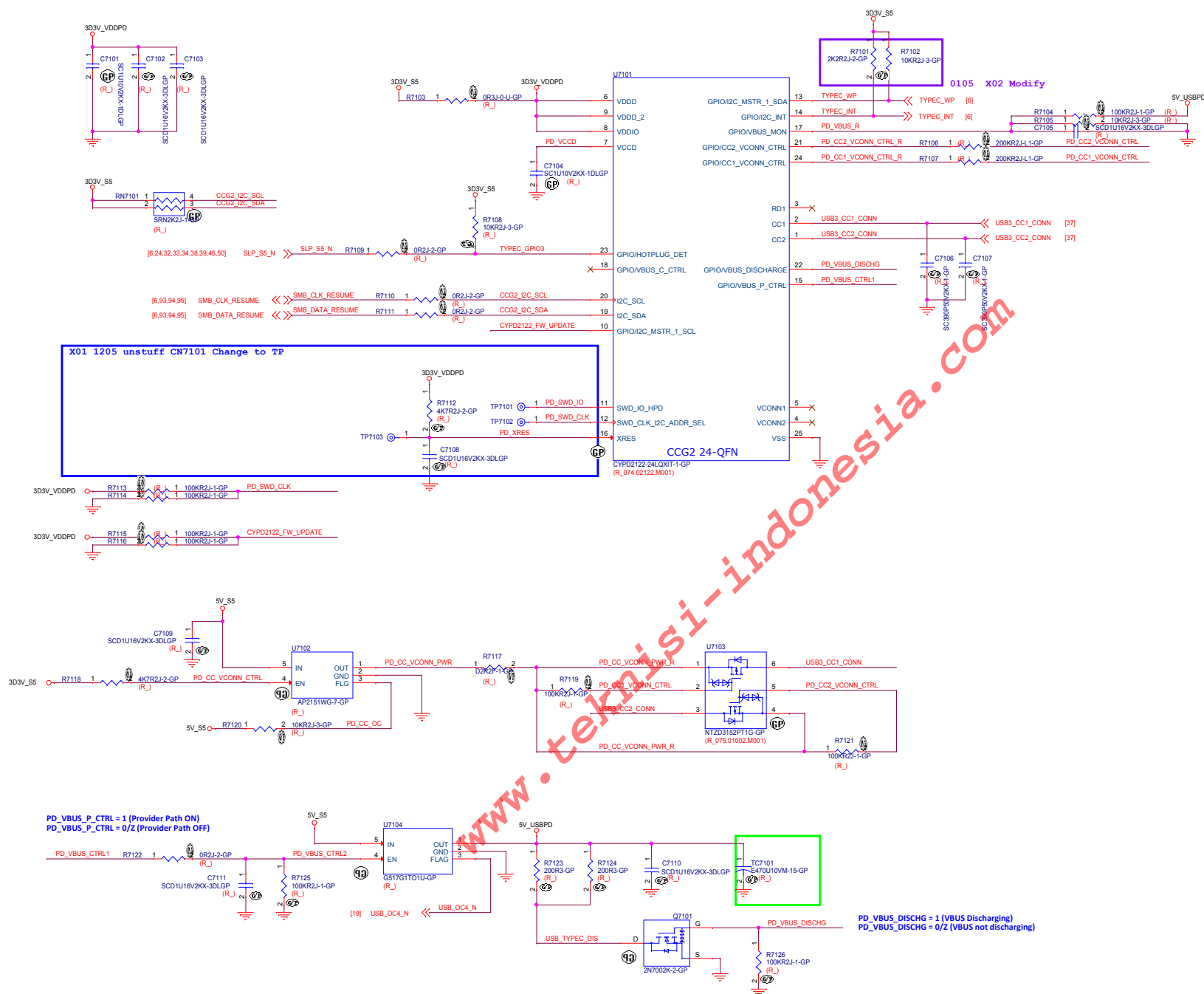
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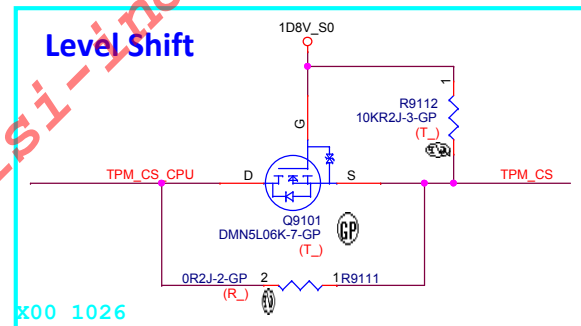
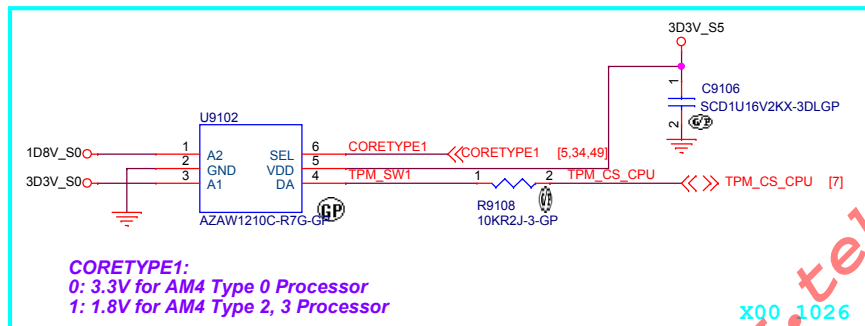
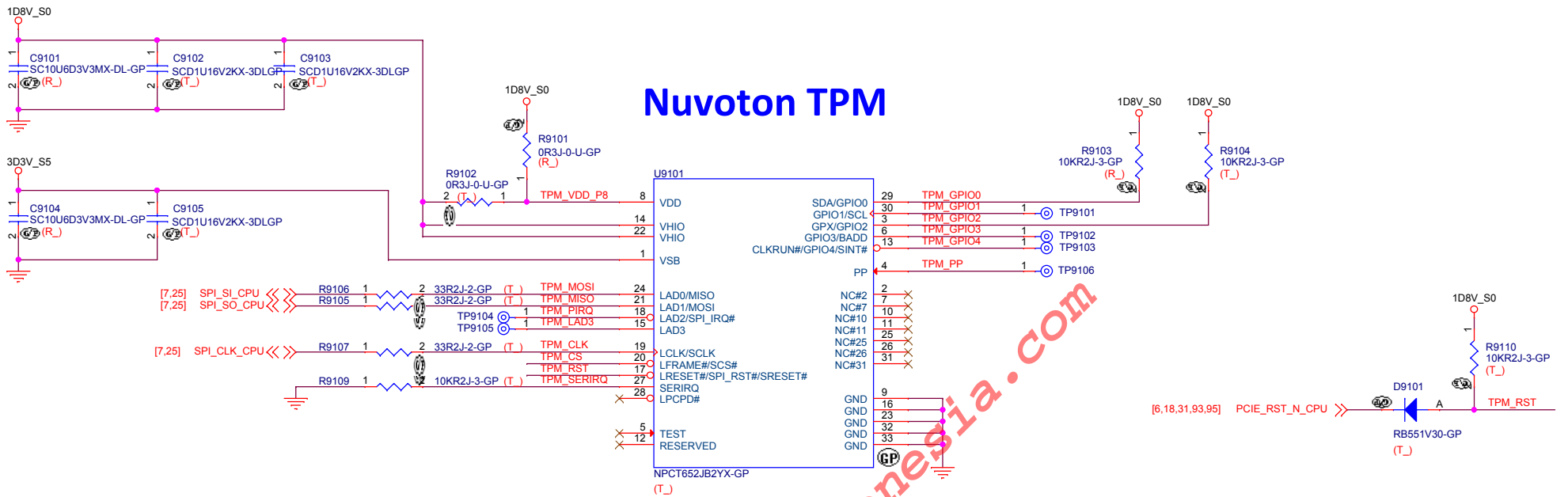
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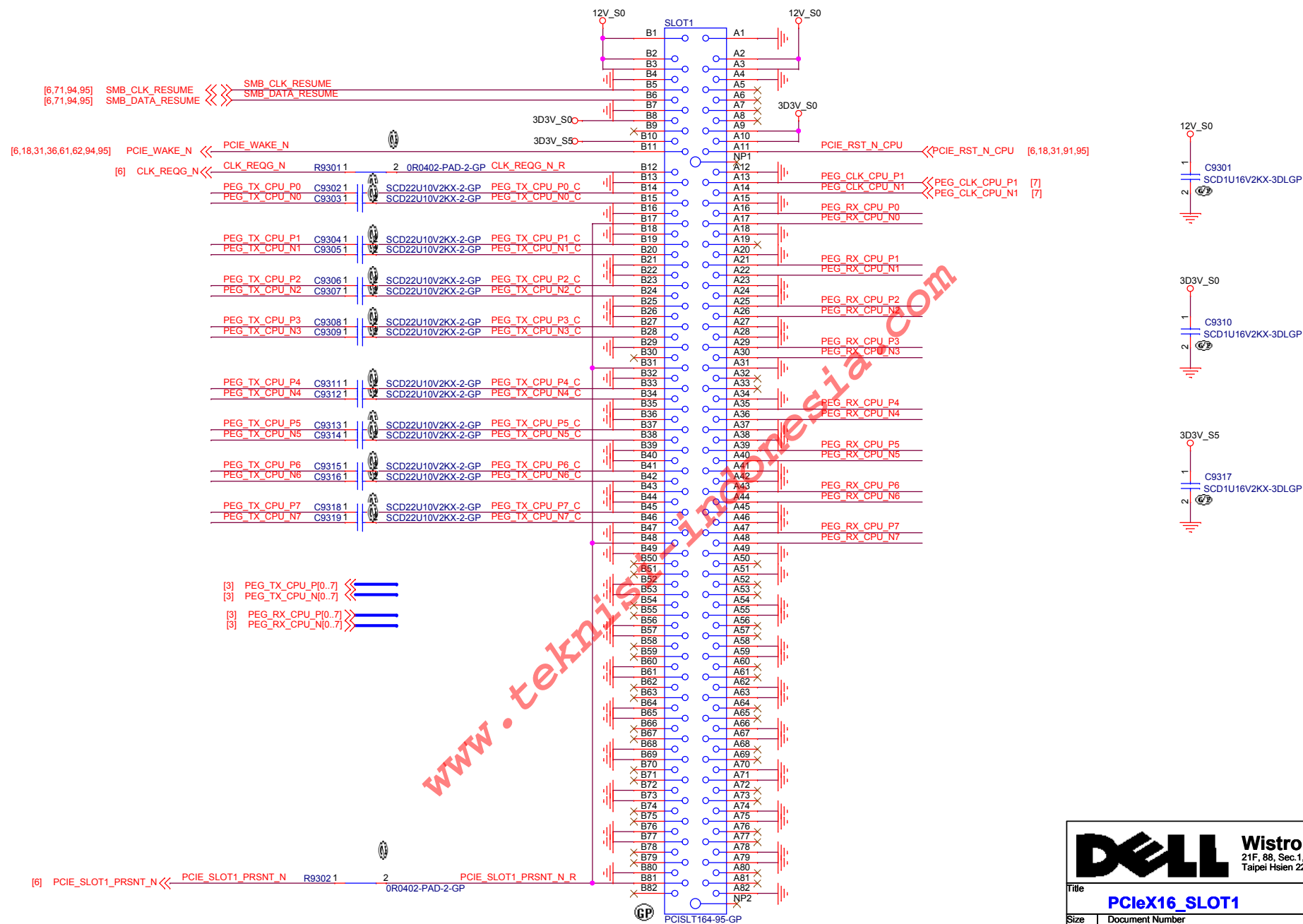


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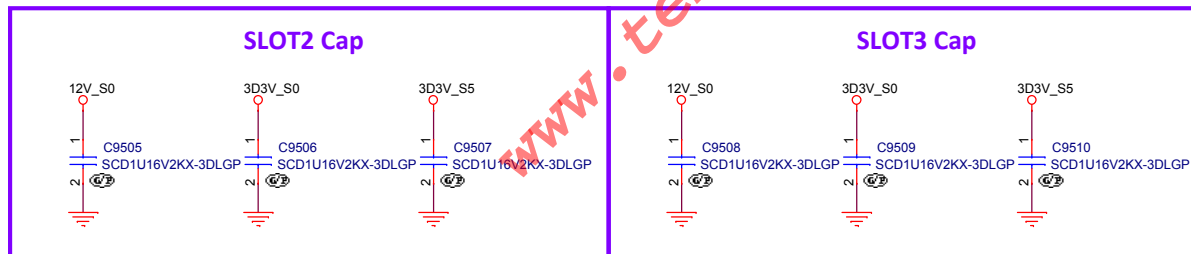
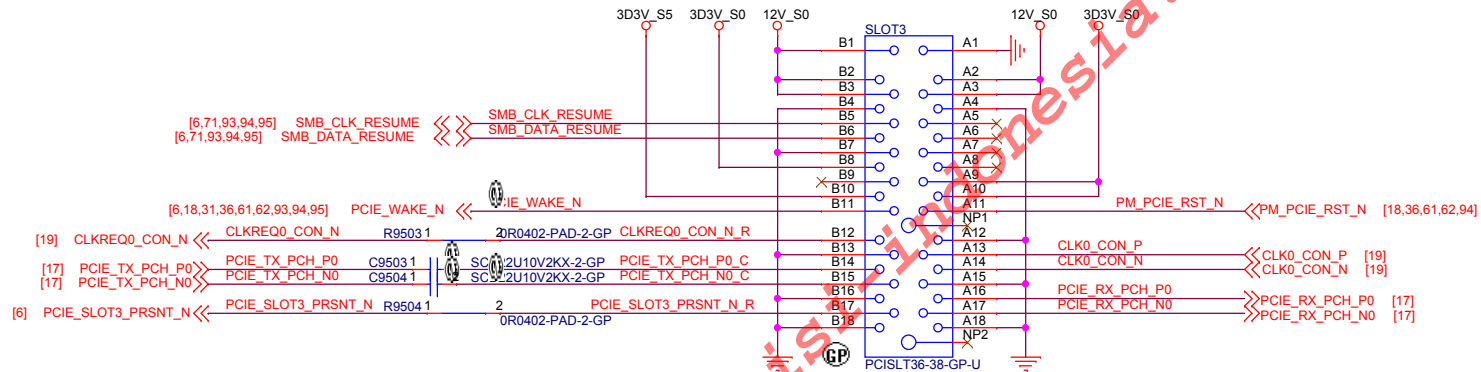
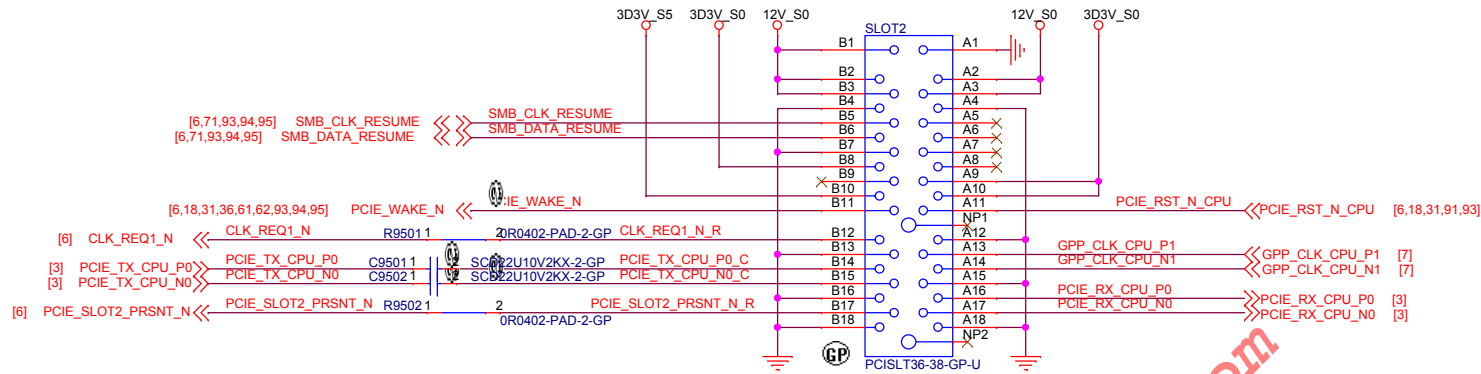
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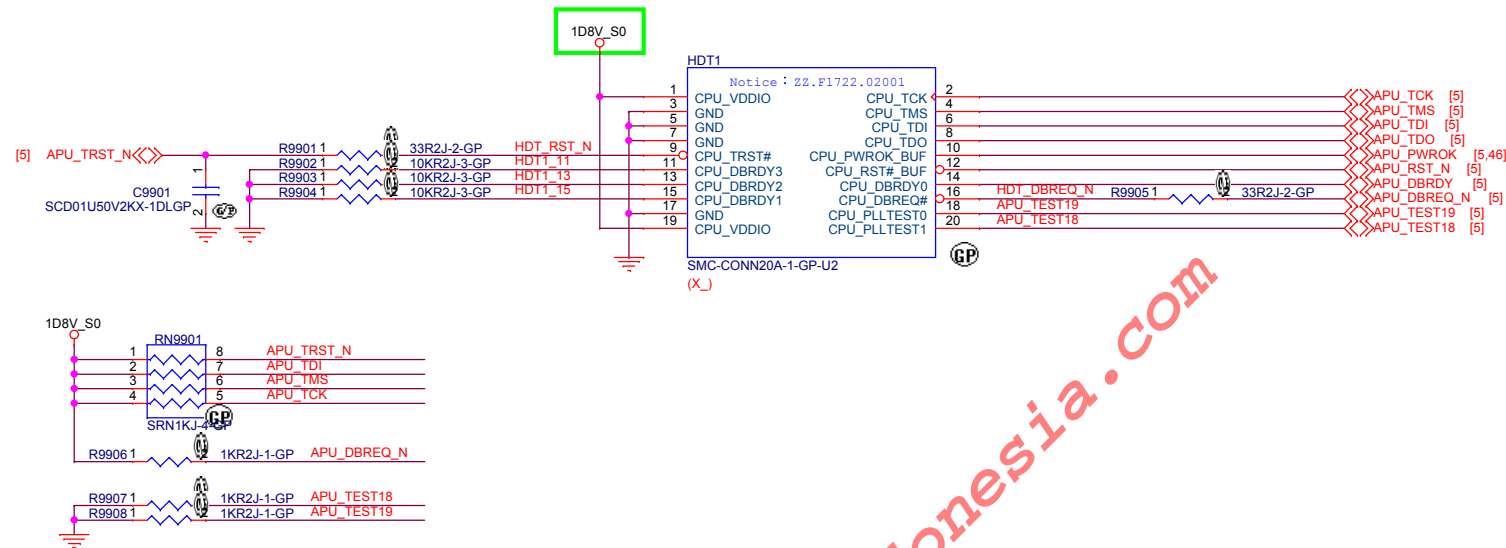
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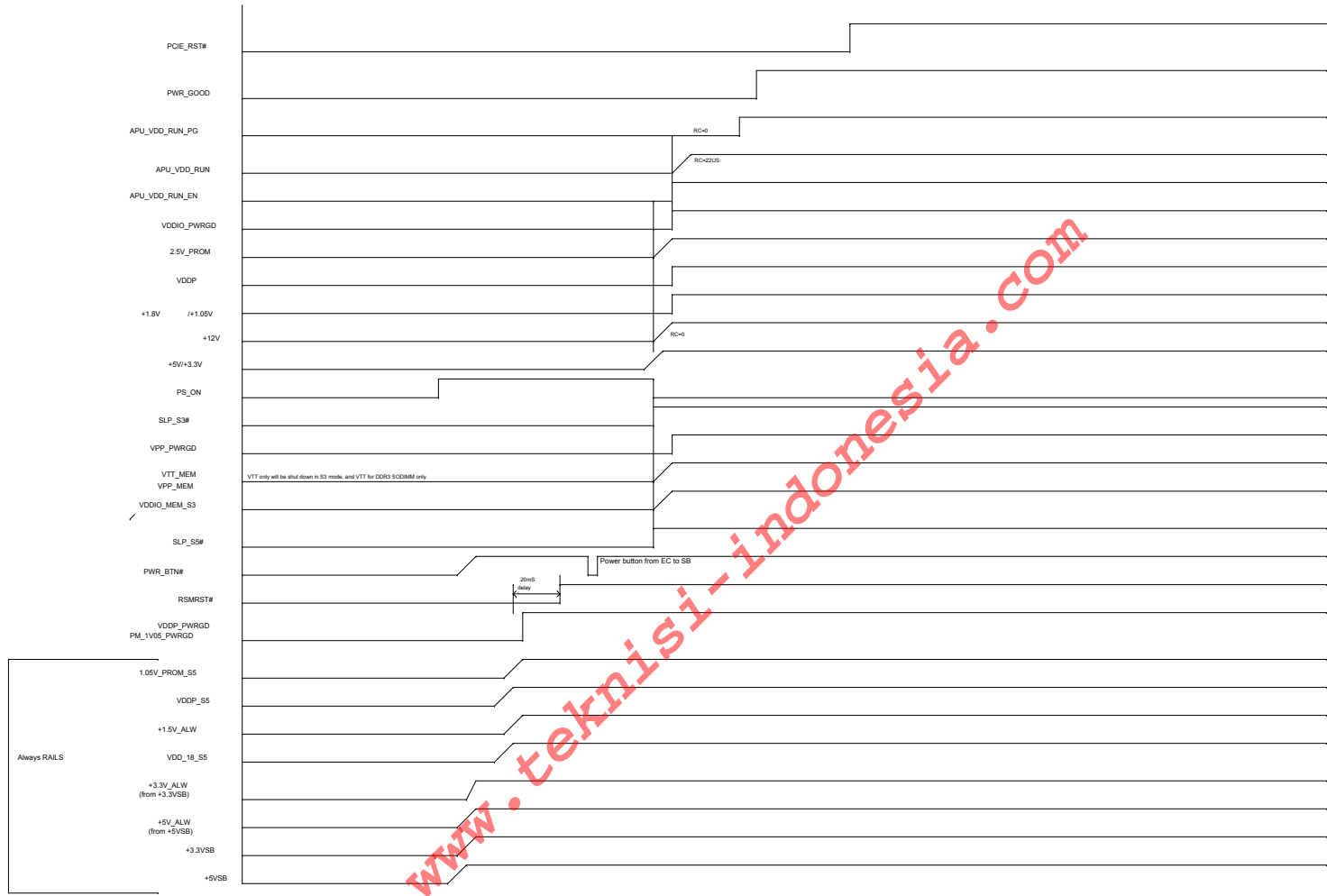
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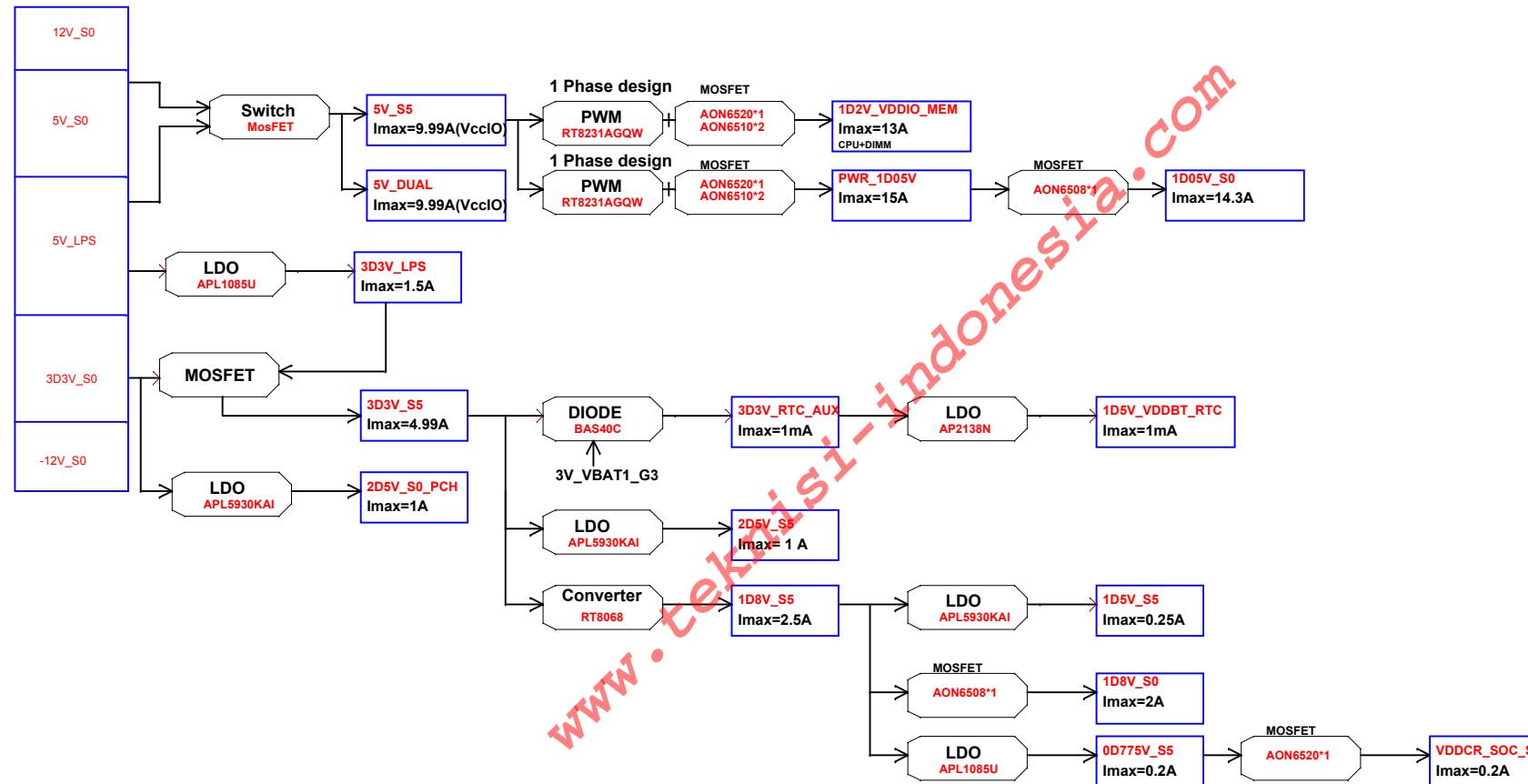
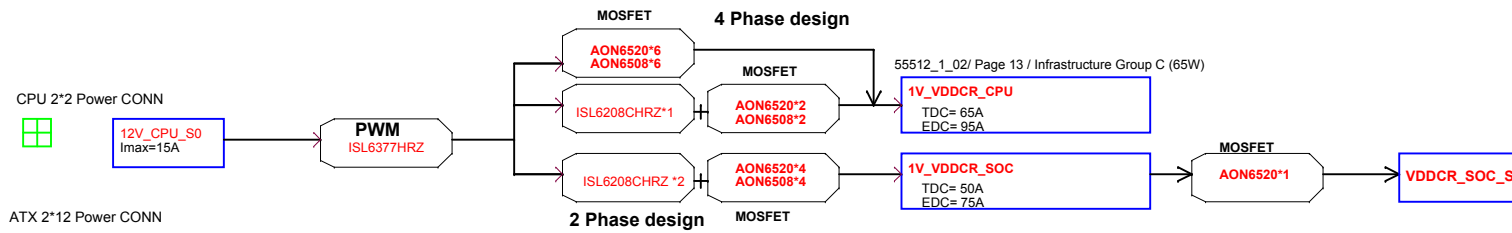
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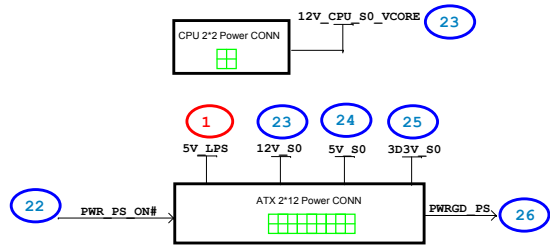
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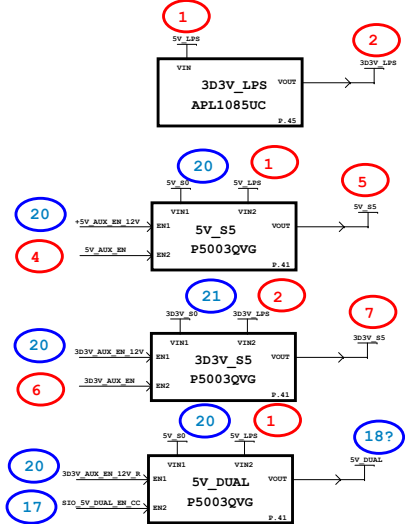
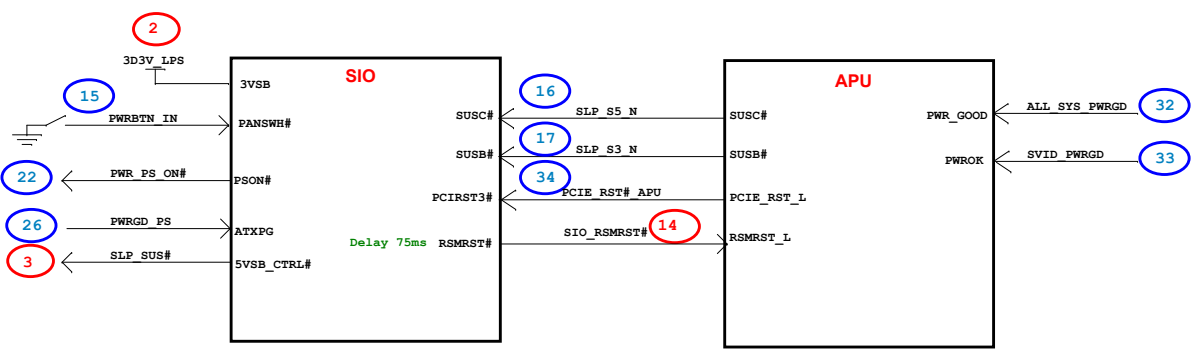
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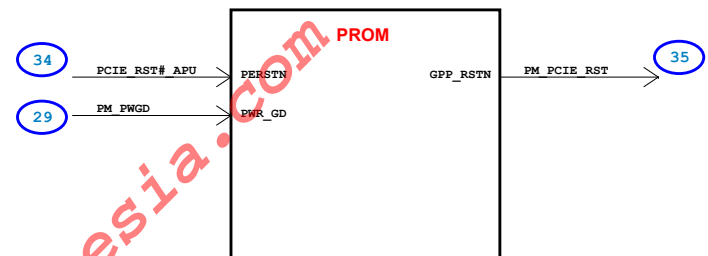
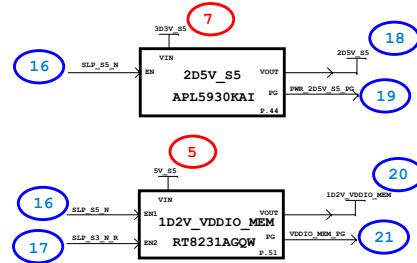




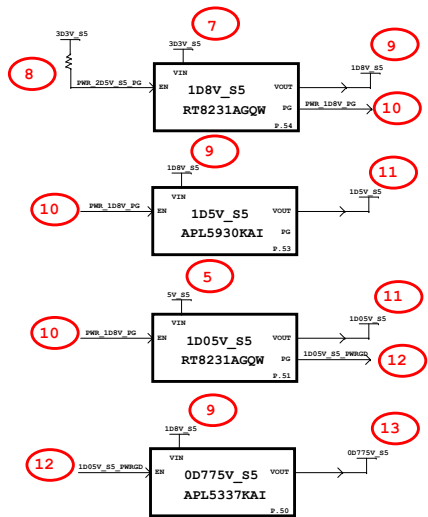
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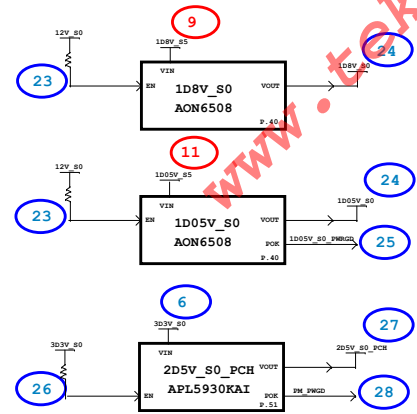
Memory voltage



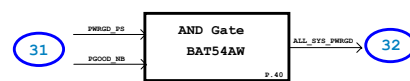
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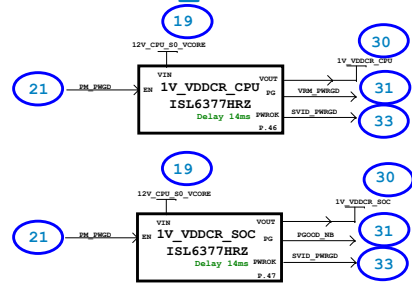
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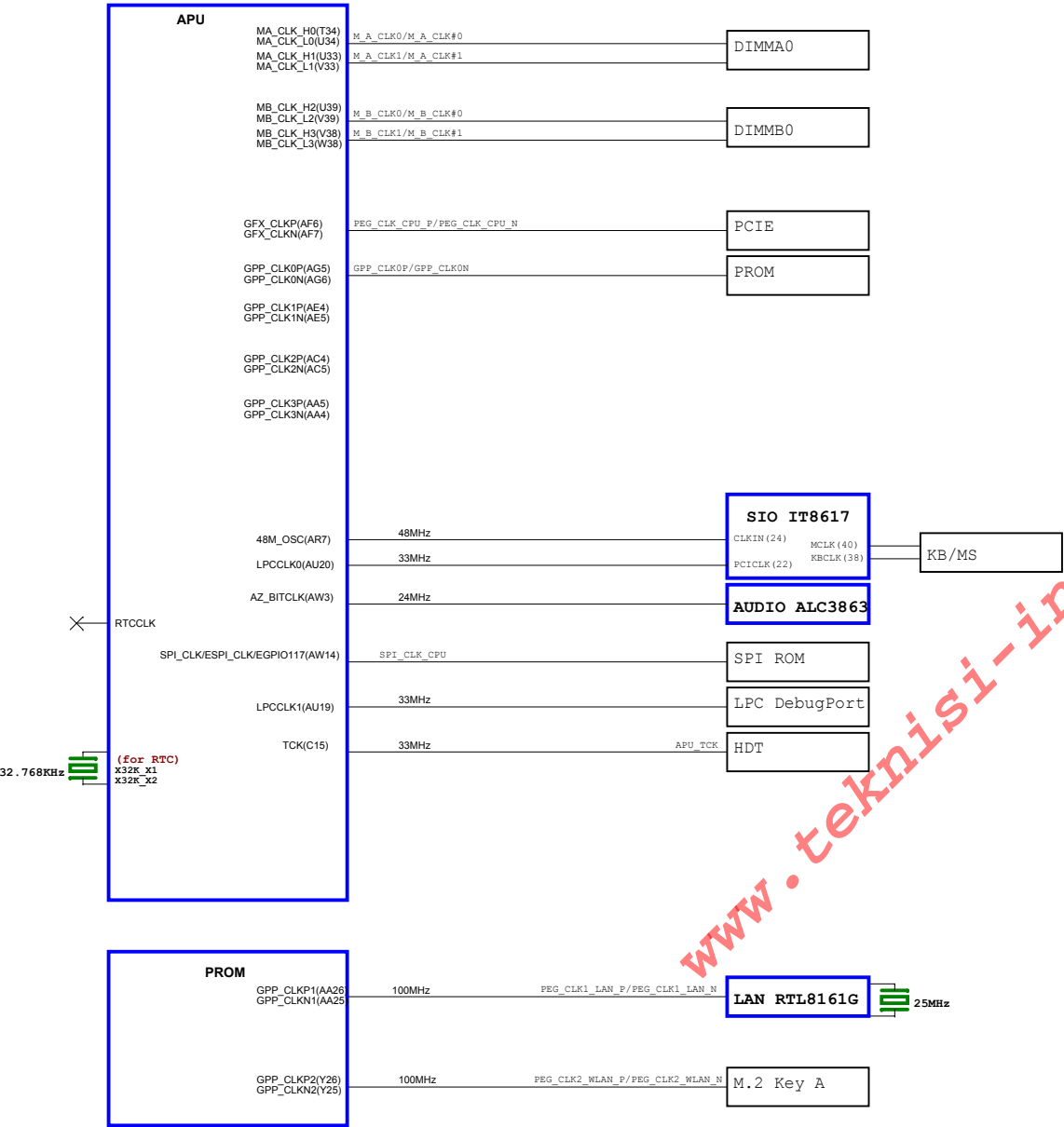
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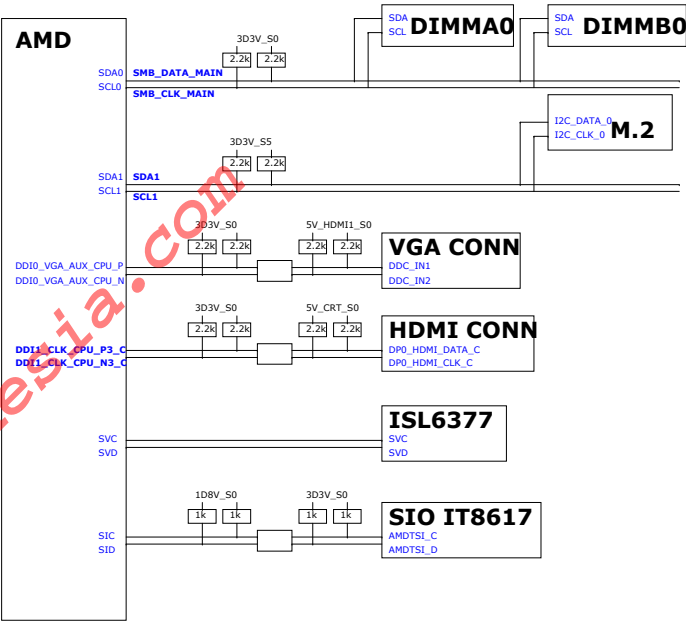
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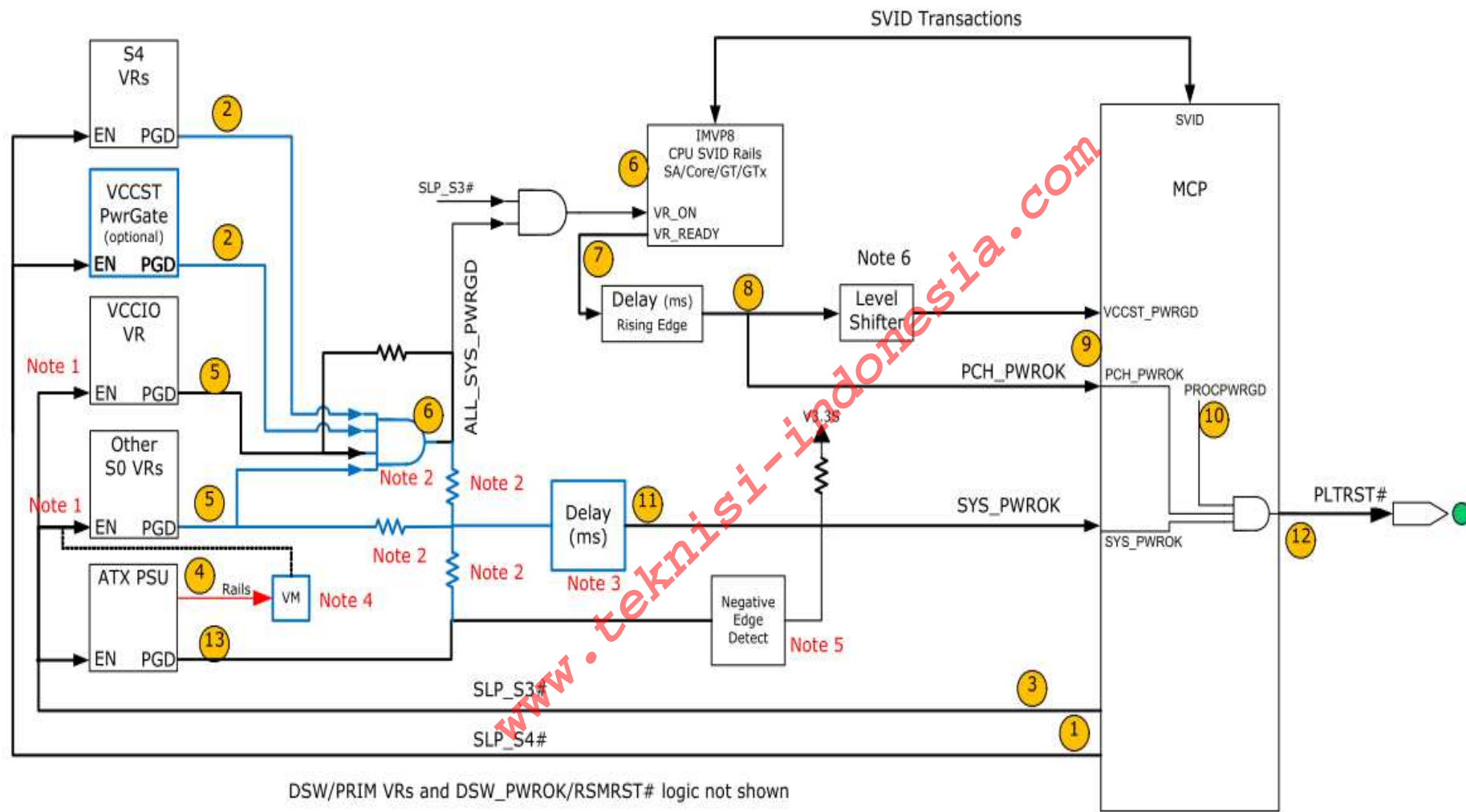


CLOCK BLOCK



SMBUS BLOCK





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